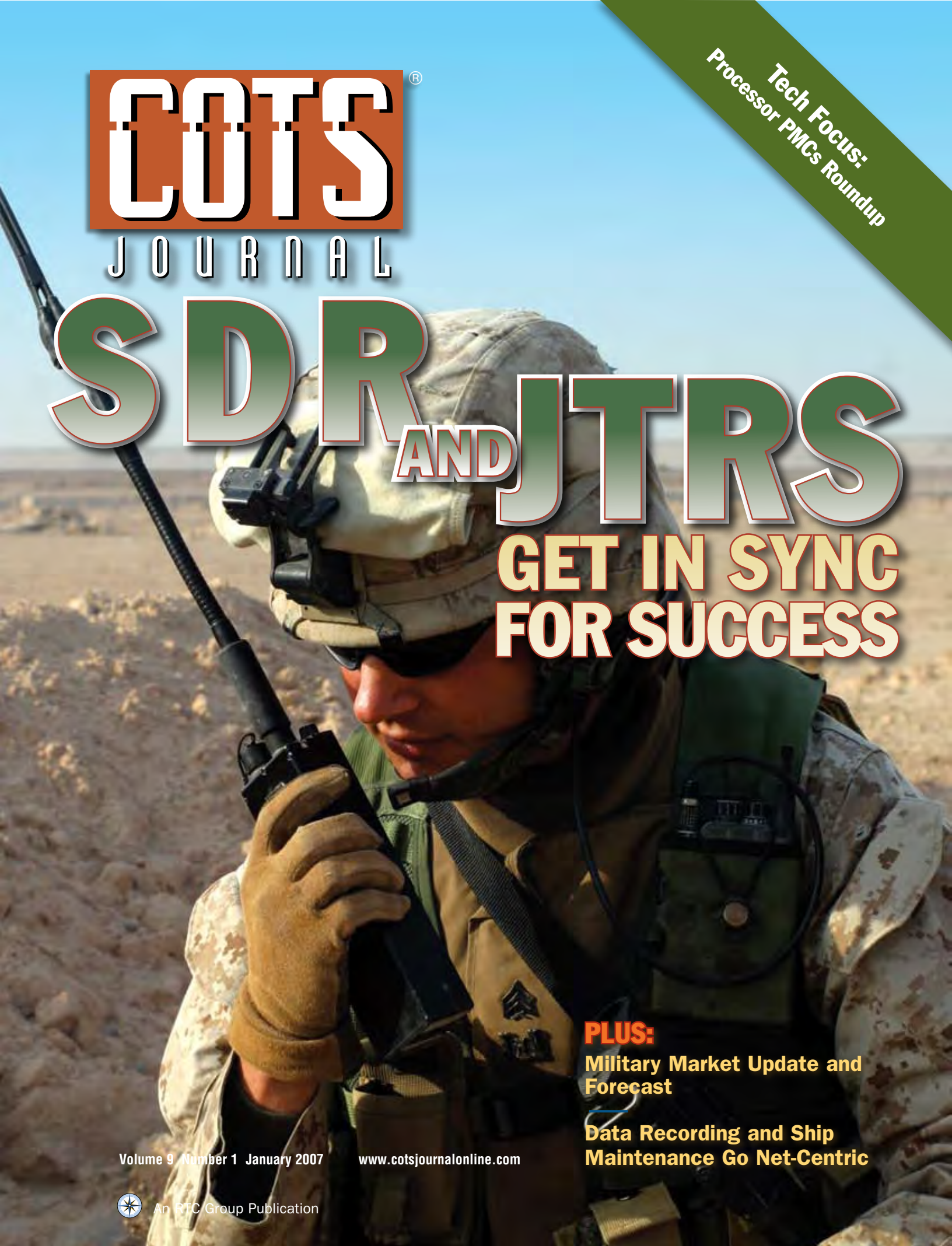

# COTS JOURNAL

Tech Focus: Processor PMCs Roundup

# SDR AND JTRS GET IN SYNC FOR SUCCESS

**PLUS:**

**Military Market Update and Forecast**

**Data Recording and Ship Maintenance Go Net-Centric**

Volume 9 Number 1 January 2007 www.cotsjournalonline.com

An RTC Group Publication







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| **COM 3** | RS–232 | NA | RS–422/485 |
| **COM 4** | RS–232 | NA | RS–232 |
| **COM 5** | RS–232/422/285 | NA | NA |
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| **LPTI** | 0 | 0 | 1 |
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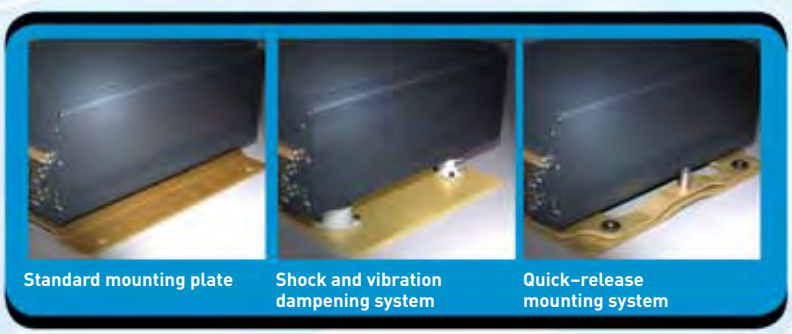

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COTS JOURNAL

# Features

January 2007 Volume 9 Number 1

## Special Feature

Software Defined Radio



## Tech Recon

Military Market Update



## System Development

Net-Centric Systems



## Technology Focus

Processor PMCs



COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

## Departments



**Coming in February...**
**...See** Page 69

**Cover Story ..... Page 14**

U.S. Marine Corps Sergeant Brandon Shofne, 2nd Combat Engineers Battalion, uses a MBITR AN/PRC-148 to radio headquarters during a weapon cache sweep in Kharma, Iraq, during Operation Iraqi Freedom. Made by Thales Communications, the radio is a predecessor to the more advanced software radios in development now. The unit is upgradeable to a AN/PRC-148 JTRS Enhanced MBITR, or JEM version—the first JTRS radio to be fielded. The JEM allows inclusion of new JTRS waveforms, such as high-capacity data, networking, and new encryption algorithms.

*DoD photo by Lance Cpl Matthew Hutchison, USMC*

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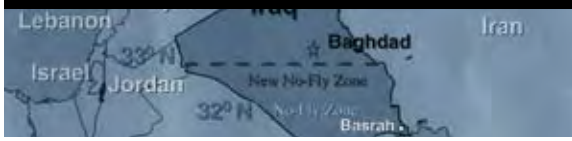
# Notebook




## The Industry from 10,000 Feet

My first industry conference was the National Computer Conference (NCC) in 1978. Every year thereafter I would attend that conference or others. Conferences would come and go as the industry changed, and my selection of conferences changed as my focus within the industry shifted. Conferences have always been a great way to keep track of what is going on in the industry. Too often though we don't realize that they provide industry data on many levels. Often we get trapped into focusing on the "Moore's Law" technology changes and don't see the bigger changes. We only see what boards or systems are using the latest, greatest chip technology with the latest speed increase. We even notice what new standards or architectures are being implemented and by whom.

Conferences tell us more than the functionality of technology and its implementation—they convey shifts on a bigger scale. The NCC supported the minicomputer market. Along came Comdex, which was the real venue for the birth of the embedded computing (remember the S-100 bus?) and PC market. At this time we also saw the introduction of conferences that focused on different elements of the industry, like communications. If we stand back and look at conferences and their pattern of success and failure, we can also get a better understanding of the more global shifts in the market. Unless we really try hard, we miss this important element when we attend a conference year after year. Our focus is too narrow and all we see are incremental technology changes.

Our most recent visit to I/ITSEC (Interservice/Industry, Training, Simulation, Education Conference—that's a mouthful) was a revelation to us. The change was probably more evident to our editorial team than it was to other attendees because we focus on system make up, not the application. We've been attending the conference for about four years. It's a great place to investigate the implementation and utilization of embedded electronics for the military and severe environment applications. Over the span of our visits we've had the ability to absorb how quickly the end use simulation market has been changing. The most recent austerity for non-essential spending by the military may have helped this. This year there seemed to be less uniformed personnel in attendance and less "in the field" training systems on display—systems designed to be deployed in rear areas with the troop. There were still small arms fire training displays and cockpit simulators, but systems seemed smaller and more compact.

It wasn't until the middle of our first day that we realized we were experiencing a major change in the simulation industry. In previous years we encountered systems containing more dedicated hardware in order to achieve the desired performance. This year the "vast" majority of the applications just used off-the-shelf flat screen displays and PCs. Although many systems stacked the PCs in racks, there was a large contingent where the ganged PCs were free standing, or even laptops. This was clear evidence that the consumer demand for life-like interactive video games along with performance demands of the PC had clearly permeated the simulation market. The critical element that suppliers are now providing to the simulation market is the man-machine interface. The includes the actuators converting physical movement into electronic signals, and the software to create the visual display and the response by the operator.

How will what was on the floor at I/ITSEC this year portend for the simulation market? This market will see more and more new suppliers as packaged software content in systems increases, reducing the cost of market entry. When you sell a quantity of a system, the application software is a one-time expense and can be modified for other product. In contrast, the man-machine interface, which is a recurring expense, will continue to be costly. Although the largest target market at this conference is the military, we've already seen a large number of systems offered for fire, police, crane operators, and so on. The range of simulation tools expands every year and we will see product offerings for virtually every market that requires some form of thought and a physical response. I don't think it will be long before every secondary school will have simulators for driver education.

Not all conferences wither and die as major market and technology shifts take place. If we look at a market from 10,000 feet rather than up close, through vehicles like conferences, we should be able to see major shifts in markets and technology. Some conferences are unable to adjust, and new ones take center stage. Others recognize the changes and adjust. I/TSEC is one of those that appears to have the ability to change as technology and the market shift. There may also be some things that the overall embedded market can learn from what is happening in the simulation market. 2007 could be a very exciting year…Oh, and Happy New Year from our *COTS Journal* team. ■■

**Pete Yeatman, Publisher**
*COTS Journal*

COTS JOURNAL

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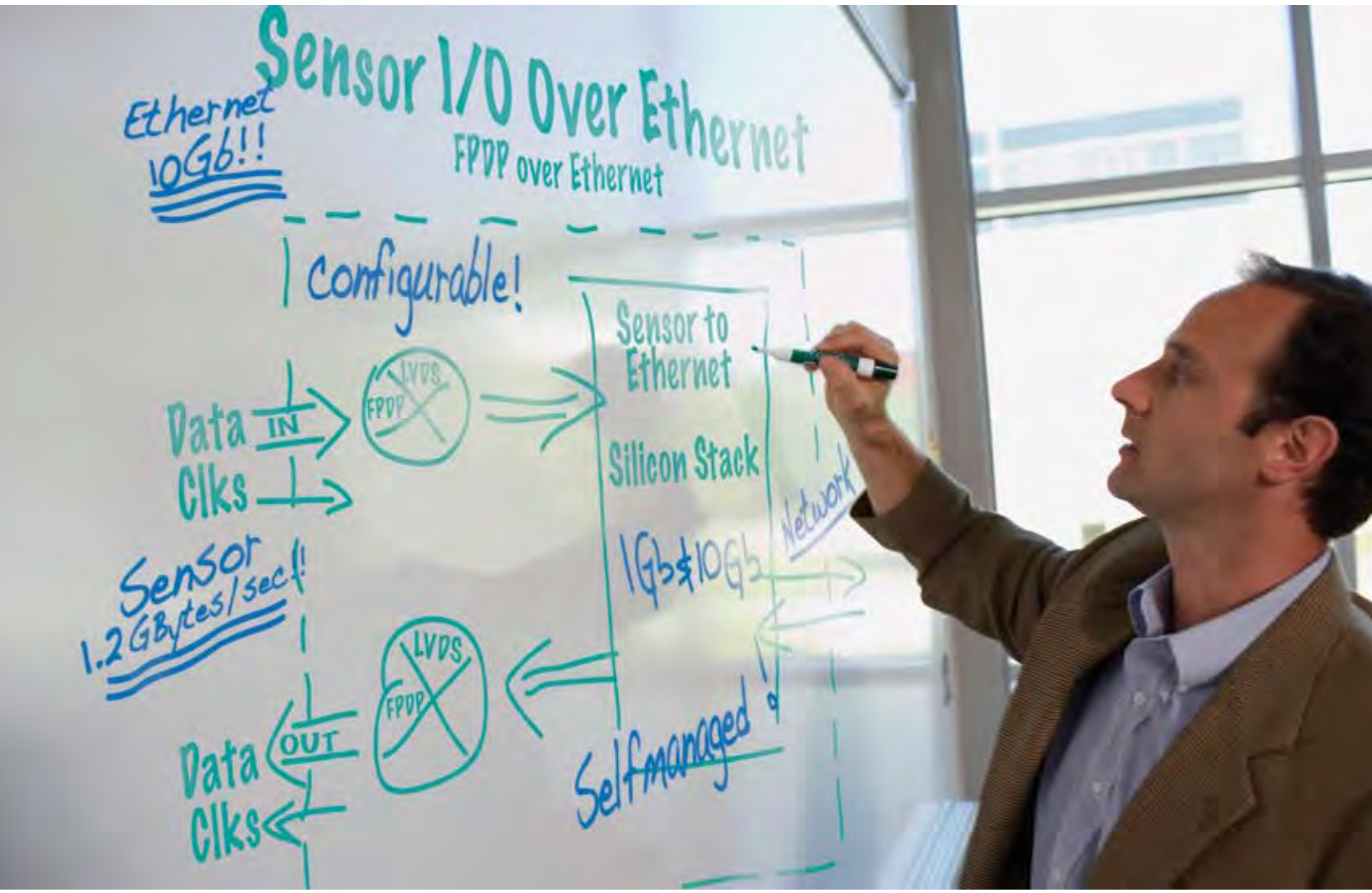


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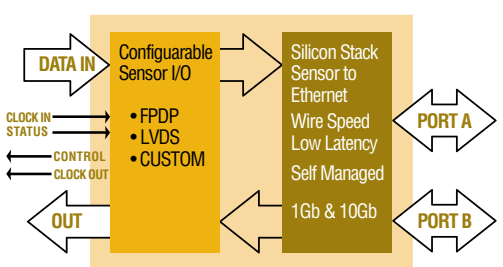


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# The Inside Track

## A Wealth of Electronics Fly Onboard F-35 JSF Lightning II's First Flight

On December 15, the F-35 Lightning II flew for the first time from Lockheed Martin in Fort Worth, TX, carrying a wealth of advanced electronics and systems. The stealthy F-35 is a supersonic, multi-role, 5th-Generation fighter designed to replace a wide range of existing aircraft, including AV-8B Harriers, A-10s, F-16s, F/A-18 Hornets and United Kingdom Harrier GR.7s and Sea Harriers. Lockheed Martin is developing the F-35 Lightning II with its principal industrial partners, Northrop Grumman and BAE Systems.

L-3 Display Systems is developing the panoramic cockpit display system for the aircraft, which will include 20 in. x 8 in. active matrix liquid crystal displays and display management computer. Among the others supplying F-35 avionics systems are: Vision Systems International providing the advanced helmet-mounted display; BAE Systems Platform Solutions making an alternative design helmet-mounted display, based on the binocular helmet being developed for the Eurofighter Typhoon; Ball Aerospace providing the Communications, Navigation and Integration (CNI) integrated body antenna suite; Harris providing the advanced avionics systems, infrastructure, image processing, digital map software, fibre optics, high-speed communications links and part of the Communications, Navigation and Information (CNI) system; Smiths Aerospace providing electronic control systems, electrical power system (with Hamilton Sundstrand) and integrated canopy frame.

Figure 1
Shown here on December 15, the F-35 Lightning II flew for the first time from Lockheed Martin in Fort Worth, TX, carrying a wealth of advanced electronics and systems.

Battery vendor Saft was chosen by Smiths Aerospace to power the aircraft. Saft provided both Lithium-ion (Li-ion) and Nickel Cadmium (Ni-Cd) batteries for the F-35 Lightning II JSF. Both batteries provide start-up power for the F-35 aircraft's Auxiliary Power Unit (APU). Smiths Aerospace supplies the Battery Charger Control Unit (BCCU) System Integrator, responsible for providing monitoring, charging and power distribution from the batteries to the aircraft.

Saft America
Cockeysville, MD.
(410) 771-3200.
[www.saftbatteries.com].

Smiths Aerospace
Grand Rapids, MI .
(616) 241-7000.
[www.smiths-aerospace.com].

## DoE Selects Data Physics' Tools for Navy Propulsion Test

A Department of Energy (DoE) research and development facility (Schenectady, NY) recently took delivery of eight 4-channel SignalCalc Ace Dynamic Signal Analyzers and twenty-two 32-channel SignalCalc Mobilyzer Dynamic Signal Analyzers, which can also function as a single 704-channel Savant system to form a comprehensive dynamic data acquisition and analysis capability to support the Naval Nuclear Propulsion Program responsible for the research, design, construction, operation and maintenance of U.S. nuclear-powered warships. After an exhaustive evaluation of available solutions, the Department of Energy selected Data Physics over the potential European suppliers as having the most complete real-time data acquisition and analysis platform, no other U.S. suppliers offered a serious challenge.

DoE's test requirements range from highly mobile 4-channel applications to a 704-channel system in the laboratory. The solution from Data Physics includes eight 4-input/2-output channel Ace analyzers on the Quattro platform and a Savant analyzer comprising twenty-two 32-input/4-output channel Abacus units. The twenty-two Abacus chassis may be used as a single 704-channel test system, twenty-two 32-channel systems and every conceivable combination in between.

Data Physics
San Jose, CA.
(408) 437-0100.
[www.dataphysics.com.].

## BAE Systems to Provide Electronic Jammers to Defeat IEDs

BAE Systems has received a $79.5 million contract from the U.S. Navy to provide Dismounted Counter Radio-Controlled Improvised Explosive Device Electronic Warfare (D-CREW) systems to meet urgent Department of Defense requirements in support of Operation Iraqi Freedom and Operation Enduring Freedom.

The contract calls for up to 3,800 wearable jammers to defeat radio-controlled detonators used on some improvised explosive devices. The wearable electronic signal-jamming systems will be used by forces in each of the military services. IEDs are the leading killers of U.S. troops in Iraq, having claimed the lives of more than 1,000 service members and wounded more than 10,000. The program is expected to be completed by October 2008. Work will be performed in Christchurch, Dorset, United Kingdom; Lansdale, PA.; and Nashua, NH.

BAE Systems
Nashua, NH.
(603) 885-2812.
[www.baesystems.com].

## General Dynamics Opens Innovation Center Focused on Warrior Systems

General Dynamics C4 Systems has opened a new initiative called the EDGE, the first facility of its kind that focuses solely on technology worn and carried by warfighters. Located at the General Dynamics facility in Scottsdale, Arizona, the EDGE has attracted interest from industry, government and academia including Arizona State University's Flexible Display Center.

EDGE member companies include Apogee Software, Inc. of Campbell, CA, Charles River

Figure 2
General Dynamics is prime systems integrator on many Army programs involving advanced technology for the warfighter including Land Warrior and the Future Force Warrior Advanced Technology Demonstrator.

Analytics of Cambridge, MA and several others. Government program management participants include PEO Soldier at Ft. Belvoir, Va.; the U.S. Army Soldier Systems Center at Natick, MA.; and the Training and Doctrine (TRADOC) Capabilities Manager-Soldier at Fort Benning, GA.

General Dynamics is prime systems integrator on many Army programs aimed at advancing technology and capabilities for the warfighter including Land Warrior and the Future Force Warrior Advanced Technology Demonstrator. General Dynamics also leads the integration effort for the U.S. Army's Mounted Warrior and Air Warrior programs. The company executes programs that are enhancing capabilities of mounted and dismounted warfighters in the United Kingdom for the BOWMAN C4I System, for Australia's Battlefield Command System (Land) known as JP 2072 and to the Royal Netherlands Navy to supply the Integrated Marine Command Information Systems (NIMCIS).

General Dynamics C4 Systems
Scottsdale, AZ.
(877) 449-0600.
[www.gdc4s.com].

## Raytheon Gets $32.7 Million Subcontract for Sea-Based X-Band Radar Support

Raytheon Company has been awarded a $32.7 million subcontract to provide sustainment support for the X- Band Radar (XBR) portion of the Sea-Based X-Band Radar (SBX). The award was made by Boeing Integrated Defense Systems, the prime contractor for the Ground Based Midcourse Defense (GMD) element of the Ballistic Missile Defense System (BMDS). SBX is a component of GMD.

Raytheon Integrated Defense Systems (IDS) will provide trained personnel for on-platform sustainment and operation of the XBR along with radar maintenance and development of spares. The contract will run through 2007, and work will be performed at the company's Missile Defense Center in Woburn, MA, Integrated Air Defense Center in Andover, MA and by Raytheon Technical Services Company on site at the SBX platform. Raytheon IDS designed and built the XBR for the BMDS, drawing on extensive sensor knowledge from its "Family of Radars." As a primary sensor for the BMDS, the XBR performs the critical functions of cued acquisition, target tracking, discrimination and engagement hit assessment.

The radar will help identify the hostile warhead from the decoys and countermeasures, providing additional capability for interceptor missiles to protect the U.S. and its friends and allies from ballistic missile attacks. Aboard the relocatable SBX, the XBR can be positioned in the ocean to support both testing and provide radar coverage for possible threat missile launches throughout the world.

Raytheon Company
Waltham, MA.
(781) 522-3000.
[www.raytheon.com].

Figure 3
Raytheon built the X-Band Radar (XBR) portion the Sea-Based X-Band Radar (SBX). As a key part of the Ballistic Missile Defense System (BMDS), the XBR can be positioned in the ocean to support both testing and provide radar coverage for possible threat missile launches throughout the world.

# COTS Websites

**www. acq.osd.mil**

## AcqWeb Provides Portal to All Things Defense Acquisition

When you're searching for information on defense acquisition it's best to start at the "top." The official Web site of the Office of the Under Secretary of Defense for Acquisition, Technology, and Logistics—dubbed AcqWeb—is a publicly accessible site and contains vast amounts of information about the Office's functions, activities and projects. Its mission is to advise the Secretary of Defense on all matters pertaining to the Department of Defense's acquisition process, research and development; advanced technology; test and evaluation; production; logistics; military construction; procurement; economic security; and atomic energy.


The Web site is a good jumping off point to information on a variety of areas from contract pricing to event info to policy changes. An "Office Navigator" provides links to all the offices related to defense applications such as Defense Research & Engineering and Acquisition Resources & Analysis. Also only a click away is the Web site for the AT&L (Acquisition, Technology & Logistics) Knowledge Sharing System (AKSS). AKSS serves as the central point of access for all AT&L resources and information, and to communicate acquisition reform. As the primary reference tool for the Defense AT&L workforce, it provides a means to link together information and reference assets from various disciplines into an integrated, but decentralized information source.

Office of the Under SecDef for Acquisition, Technology, and Logistics, Washington, DC. [www.acq.osd.mil].

# Special Feature

Software Defined Radio

# SDR and JTRS Starting to Get in Tune

In 2006, the JTRS reorganization was unveiled, as the JPEO moved to get the program back on track and some first products were delivered. At the same time, the flow of software defined radio hardware components, software and development tools continued apace.

David B. Cotton
Contributing Editor

*COTS Journal* first started reporting on Software Defined Radio in its January/February 2000 issue and, since then, has continued to update developments in the field with numerous timely articles plus an annual review. Seven years later it's reasonable to ask, "Is 2007 the year when it will finally come to fruition? What can we expect?"

## JTRS Reorganization

The year 2005 was one of great uncertainty for the U.S. DoD's Joint Tactical Radio System (JTRS). Late in 2004, after recognizing that the program was plagued with delivery delays, cost overruns and threats of budget cuts, the DoD moved its management from the original Joint Program Office (JPO) to a new Joint Program Executive Office (JPEO). Most of 2005 and part of 2006 was spent by the JPEO in both understanding the scope of their problems and developing a plan to fix them.

When the new JTRS plan came out in the first half of 2006, some projects had been cut or delayed, much had been rearranged or reorganized, and some new things had been added (Figure 1). Among the cuts was the number of waveforms—from the originally planned 32 to six—although some or all of the others may be considered later. And, among the additions, it appears that much more attention will be paid to integrating the

**JTRS Product Line Overview**

- **Ground Domain**
  - Ground Mobile Radio (GMR) (formerly Cluster 1)
    - Support requirements for Army and USMC Ground Vehicular Platforms
  - Handheld/Manpack/Small Form Factor (HMS) (Formerly Cluster 5)
    - Support requirements for JTRS handheld and manpack units and forms suitable for integration into platforms requiring a Small Form Fit radio
- **Airborne Domain**
  - Airborne and Maritime/Fixed Station
    - Support requirements for airborne (including rotary wing), maritime, and fixed station platforms for all Services
  - Multifunctional Information Distribution System – JTRS (MIDS-J)
    - Migrate the current MIDS-Low Volume Terminal (LVT) to MIDS-JTRS compliance producing the next generation data link and communication terminal for joint and coalition tactical platforms
- **Network Enterprise Domain**
  - Includes former JTRS Joint Waveform Program Office
    - Responsible for the waveform development, cryptographic equipment applications, architecture and integrity of JTRS and common network services
- **Special Radios**
  - JTRS Enhanced Multi-Band, Inter/Intra Team Radio (MBITR) (formerly Cluster 2)
    - Managed by Special Operations Command (SOAL-IIS-PMC4)
    - Support requirements for handheld radios for Army, Navy, Marine Corps and Air Force Special Operations Forces

Figure 1

Joint Tactical Radio System Product Line Overview, as per JPEO JTRS presentation of May 3, 2006.

JTRS into the military's Global Information Grid (GIG). Almost concurrent with the new plan were announcements that the DoD had approved the JTRS budget and signed an Acquisition Decision Memorandum (ADM) officially approving the "way ahead" strategy. Not too long thereafter, the JPEO announced an update to its Software Communications Architecture (version 2.2.2).

Hopefully, this new plan will allow the JTRS program to move ahead smartly. But, even assuming that the JPEO plan is good, that it resets the baseline of the program and that it solves most of the problems, there still appears to be one major area of concern that has yet to be addressed. According to several well-placed and knowledgeable SDR observers, the JPEO still needs to face up to the issue of a valid business model for waveforms.

These sources point out that in order for SDR to be viable in the long term, vendors need to be able to understand how to make money. And, in the waveform field, there appear to be two choices. Either let the waveforms be a commodity and allow the vendors to make money on the hardware, or commoditize the hardware and let the vendors make their money on the waveforms. At this time, unfortunately, the government appears to want to make both the waveforms and the hardware into commodities, and that just will not work. Since the problem is well known to the JPEO, let's hope that is gets solved soon.

## On the Commercial Side

In addition to the JTRS JPEO, major stakeholders in Software Defined Radio include the prime contractors for the various JTRS programs and their subcontractors, plus a whole host of companies and related organizations located around the world that are developing hardware, software or other tools designed to facilitate the development, production and deployment of SDR devices. Not surprisingly, outside of the United States, the largest concentration of these stakeholders is based in Canada. Possible SDR customers, in addition to the U.S. military and their allies, include public safety organizations worldwide and telecommunications companies and their users.

In 2006, much of the industry news came from the vendors of software and other development tools, including platforms and systems that could support the development of software radios. For example, the Communications Research Centre Canada (CRC) upgraded an existing offering by announcing SCARI Software Suite 2007, a Component-Based Development (CBD) environment for SDR, which includes the SCA Core Framework and a completely redesigned CBD tool set.

Lyrtech, another Canadian organization, introduced its Small Form Factor (SFF) SDR Evaluation Module, SFF SDR Development Platform and SFF SCA Development Platform. Their development platforms are designed to address the needs for a highly portable SDR for military, public safety and commercial markets.

Spectrum Signal Processing—still another Canadian company—announced the availability of its flexComm SDR-4000 Tactical Military Communications (MILCOM) Rapid Deployment Platform (TMRDP). This platform equips quick response teams with an integrated platform designed for the rapid development and deployment of tactical MILCOM applications. The off-the-shelf SDR-4000 TMRDP provides full "RF to Ethernet" functionality of an SDR with support for the SCA in a single 19" rack. It integrates Spectrum's high-performance SDR-4000 wireless modem, a DRT4001 RF front-end by Digital Receiver Technology (DRT), a GPS receiver and the software necessary for tactical MILCOM deployments.

Green Hills Software weighed in with an enhanced platform for SDR and used it in a demo of network-centric operations for the AMF component of JTRS. The enhanced platform provides support for Spectrum Signal Processing JTRS platforms, the Lyrtech Small Form Factor SDR development platforms for SCA and non-SCA radios previously discussed, SCA Technica's High Assurance Wireless Computing System (HAWCS) and ISR's JTRS SDR kit. It also supports the SCA operating environment and development tools from CRC (SCARI), PrismTech, Zeligsoft, Harris, OIS and Telelogic (formerly I-Logix).


Figure 2

The AN/PRC-148 JEM radio from Thales Communications is used to equip security forces, civil engineering and tactical air control personnel.

On the hardware side, in November, Thales Communications was awarded a contract by the Air Force for more than 1,200 of their AN/PRC-148 JEM radios (Figure 2) to equip security forces, civil engineering and tactical air control personnel. Thales claims that the AN/PRC-148 JEM—JTRS Enhanced Multiband Inter/Intra Team Radio (MBITR)—is the first JTRS radio certified for compliance with the Software Communications Architecture (SCA). Over 80,000 older models of the non-JTRS MBITRs are already in the field being used in Operation Enduring Freedom, Operation Iraqi Free-

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dom and the Global War on Terrorism.

Harris received a contract for their Falcon III dual Vehicular Adapter Amplifier (VAA) systems, the AN/VRC-110, which include the AN/PRC-152(C) handheld radio (Figure 3). Subsequently, they announced that the AN/PRC-152(C) had received SCA-certification from the JTRS JPEO in addition to being NSA-certified. Harris has over 3,000 of these radios in service and expects over 17,000 to be in the field by the summer of 2007, making it the first widely fielded tactical radio to receive SCA certification. Meanwhile, over the course of the last year, Pentek introduced their 7140 and 7142 software radio transceiver PMC modules, the 6821-422 215 MHz A/D-converter and the RTS 2504 real-time data recording and playback platform (Figure 4).

Figure 3

Harris Corporation's AN/PRC-152(C) handheld radio has received SCA-certification from the JTRS JPEO in addition to being NSA-certified. Over 3,000 of these radios are in service and Harris expects that more than 17,000 to be in the field by the summer of 2007.



## So, Where Is SDR Going?

Although SDR's roots are in the U.S. DoD's perceived need for better military communications, and first shipments of JTRS radios are beginning to be delivered, for a while the field has been showing signs of a potential to be much wider. Several events help to illuminate this feeling. At a recent SDR Forum conference, Zeligsoft announced that its tool suite now provides immediate benefits to projects that focus on achieving radio interoperability across European military forces and security agencies. This supports the contention of Lee Pucker of Spectrum Signal Processing and the SDR Forum that we will soon be seeing a proliferation of SCAs targeted at different markets.

During this past year, the SDR Forum released a 98-page report on SDR Technology for Public Safety. That document's Executive Summary begins as follows: "Public safety communications today are characterized by a patchwork of separate, often incompatible systems with widely varying capabilities in communi-

cating between and amongst systems and user radios. Software defined radio (SDR) capabilities provide a key component of the solution to interoperability as well as increased flexibility and ability to adapt to evolving technologies."

When one adds the market potential that SDR holds for personal cellular communications to the existing worldwide markets for military and public safety communications, the future can look quite rosy and expansive. But, it is not without problems. Like the personal computer field in the not too distant past, technologies are moving so fast that new hardware products appear to be obsolete by the time they finish production. And, both the military and public safety fields will pose significant funding issues before a majority of the potential users can field SDR products.

Rodger Hosking, V. P. of Pentek, summarizes the near-term future as follows, "Vendors in the software radio market face many challenges and opportunities. Rapidly evolving technology in data converters, FPGAs and memory devices compress product market timing windows, thus forcing vendors to develop efficient new product development strategies with shorter design cycles. Designing open architecture products with high-density analog and digital circuitry requires expertise in packaging, layout and shielding. Software drivers, libraries and development tools for products containing increasingly complex devices mandate a tradeoff between high-level tools that are easy to use and access to low-level resources often necessary for optimizing performance." ■■


Figure 4

Pentek's RTS 2504 real-time data recording and playback platform. It is an example of a ready-to-use instrument consisting of Pentek boards installed in a chassis. It includes Pentek's SystemFlow Software Development Suite with a GUI, a real-time API, PC-host API, libraries and examples.

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# Special Feature

Software Defined Radio

# Software Communications Architecture: From JTRS to the Embedded World

Currently, the philosophy of the SCA has been identified with military radios. However, it also holds the potential to play a role in countless applications in our daily lives, from public security to consumer electronics.

Claude Bélisle, Vice President of Satellite Communications & Radio Propagation
Communications Research Centre Canada (CRC)

Software Defined Radio (SDR) came about with the development of faster signal processors—those capable of handling the data flows of modern telecommunications systems. By the end of the 1990s, software was already well established in numerous embedded systems and there was simply no return to the analog world. Moore's Law was taking over, with more and more analog signal processing being done in software.

There's no disputing that the use of software in radios is now here to stay. The question now is just *how* will this software be implemented? Initially, software was developed around hardware architecture and was adapted to fit the design. The software developer was told exactly how many Field Programmable Gate Arrays (FPGAs) and Digital Signal Processors (DSPs) there were on the board, the communications mechanism between each processor and even the pin numbers that needed to be addressed. This led to the development of very specific software with limited portability, driving up development and maintenance costs.

And so there emerged a craving for flexibility. Developers of SDR began working toward scalable software systems that could offer easy upgrades, as opposed to constantly redesigning the wheel. As with so many other systems, standardization promised to lower costs as companies could now obtain off-the-shelf products, manufactured for multiple applications or buyers. Mass production could reduce cost, and in a market where volume is often key to cost reduction, it became imperative to find a standard upon which the community could develop.

## SCA – Putting the Pieces Together

In the mid-1990s, the U.S. Department of Defense contracted the development of a specification that would serve as the binding between the software and the hardware. This specification would ensure that the software could be written almost independently of the hardware platform, so it would be relatively easy to port from platform to platform. The reverse would also apply—the hardware developed based on the specification would be able to run a multiplicity of software applications. The commissioned specification, named the Software Communications Architecture (SCA), aimed to (1) facilitate the use of COTS technology in an attempt to reduce development and maintenance cost; (2) minimize the effort required to port the software from one platform to another, for hardware upgrades or for different radio vendors; and (3) reduce the development time for new applications through the reuse of software developed for other projects.

The SCA was created to isolate the development of applications from that of the hardware. It accomplished this by providing a structured approach for loading, configuring, starting and stopping applications. Since its conception, the SCA has certainly gained momentum. Initially, it was usable only by large development teams with deep pockets. In 2002, however, the Communications Research Centre Canada (CRC), a fed-

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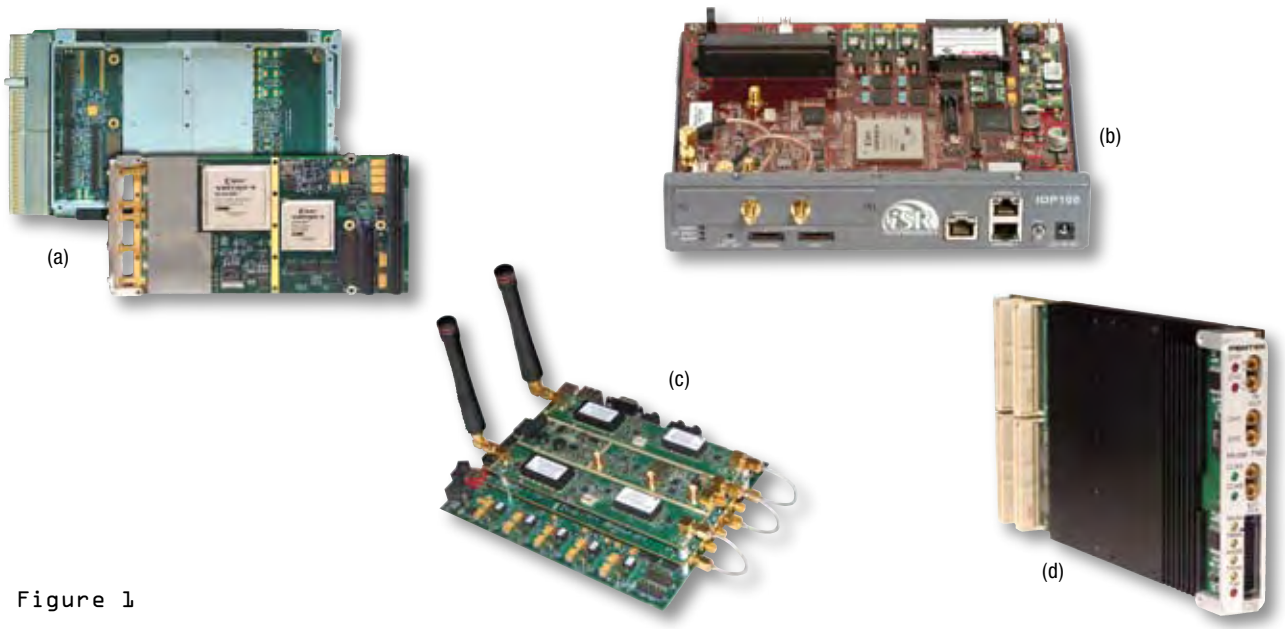


Figure 1

Examples of some SCA-enabled platforms: (a) flexComm SDR-4000 from Spectrum Signal Processing; (b) IDP-100 from ISR Technologies; (c) SFF from Lyrtech; and (d) 7140 from Pentek.

eral telecommunications laboratory, leveled the playing field by offering the first open-source version of the SCA. Today, a complete industry has now been developed around this specification, offering SCA-enabled hardware platforms and development tools. The long-awaited objective has now been met.

A number of SCA-enabled platforms are commercially available off the shelf, from a multitude of vendors such as Spectrum Signal Processing, ISR Technologies, Lyrtech and Pentek (Figure 1). The SCA offers a complete framework for managing the deployment and configuration of applications. With its underlying CORBA, it also manages the communications mechanism between the different software and hardware components. Thus, developers can focus much more rapidly on the development of their applications. There is no need to fully understand the characteristics and design of the hardware platform, as the SCA abstracts most of it from the developer. This abstraction becomes more and more important as the complexity of the platforms keeps increasing with new-generation signal processors: high-speed analog-to-digital converters, digital up- and down-converters, FPGAs, DSPs, General-Purpose Processors (GPPs) coupled with various communications bus and RF modules interfaces.

## The SCA and Software Development

The SCA is also transforming the world of applications development. The introduction of the SCA made it easier for the embedded market to shift the design approach from platform specific to a Component-Based Development (CBD) approach. Here the system is represented by an assembly of software components linked together according to a set of rules and behaviors specified, in this case, by the SCA. By abstracting the platform-specific code from the signal processing algorithms, it becomes much easier to reuse the software components from one project to another or from one platform to another. Making modifications to one component can also be done with minimal impact on the rest of the software code. Significant time and cost-savings can be realized as applications can now be developed by assembling a series of predefined, independent building blocks.

As promising as it looks, adopting a new design approach requires some time to ramp up the learning curve. The SCA, proposing a significant design shift to offer increased flexibility and portability, is no exception. While this may have been a major impediment for the early adopters of the specification, it is now a non-issue. Software tools are now commercially available, isolating the developers as much as possible from the SCA itself and thus greatly reducing that learning curve. With some of these tools, in fact, it becomes simpler and more effective to design along the SCA specification than to try to do it with a proprietary architecture. Features such as SCA-design templates, graphical representation of the components and applications, real-time SCA-design validation and automatic SCA-specific code generation help to ensure error-free designs and minimize development time.

The unique flexibility of the SCA design approach and the associated development tools is evident in the SCARI Software Suite developed by Communications Research Centre Canada (CRC). An integrated development environment for SDR technology, SCARI is already used by major hardware and software manufacturers for an array of commercial offerings using different processors and operating environments. At the heart of SCARI lies the

SCARI++, an implementation of the SCA Core Framework specifically designed for embedded systems.

Combined with the SCA Architect and Radio Manager, two tools for the development and monitoring of SCA platforms and applications, the resulting SCARI Suite aims to minimize learning curves and greatly simplify the overall SDR development cycle. The SCARI Software Suite offers a glimpse of an emerging industry, one that uses the SCA implementation itself to offer a complete solution to the traditional challenges of product development (Figure 2).

## Taking the SCA Beyond Military Radios

Today, we are starting to see the makings of a paradigm shift in embedded system development, one that could touch innumerable applications in our everyday lives. So far, the philosophy of SCA has been identified with military radios. Initially designed for the U.S. Joint Tactical Radio System (JTRS), the SCA has now been adopted by many other allied military organizations. Taking a closer look at the SCA specification, however, one can see that very little in it is directly related to military radios, and even to radio at all. The developers of the specification had a vision that would take their concept beyond a restricted set of applications. The SCA specifies a set of rules and behaviors for the development, deployment and configuration of applications and signal processing platforms. A new generation of SCA products promises to open the doors to an even wider range of applications.

When looking at other domains of applications, public safety and first responders are the obvious candidates. When converging on an emergency scene, police, firefighters and paramedics from

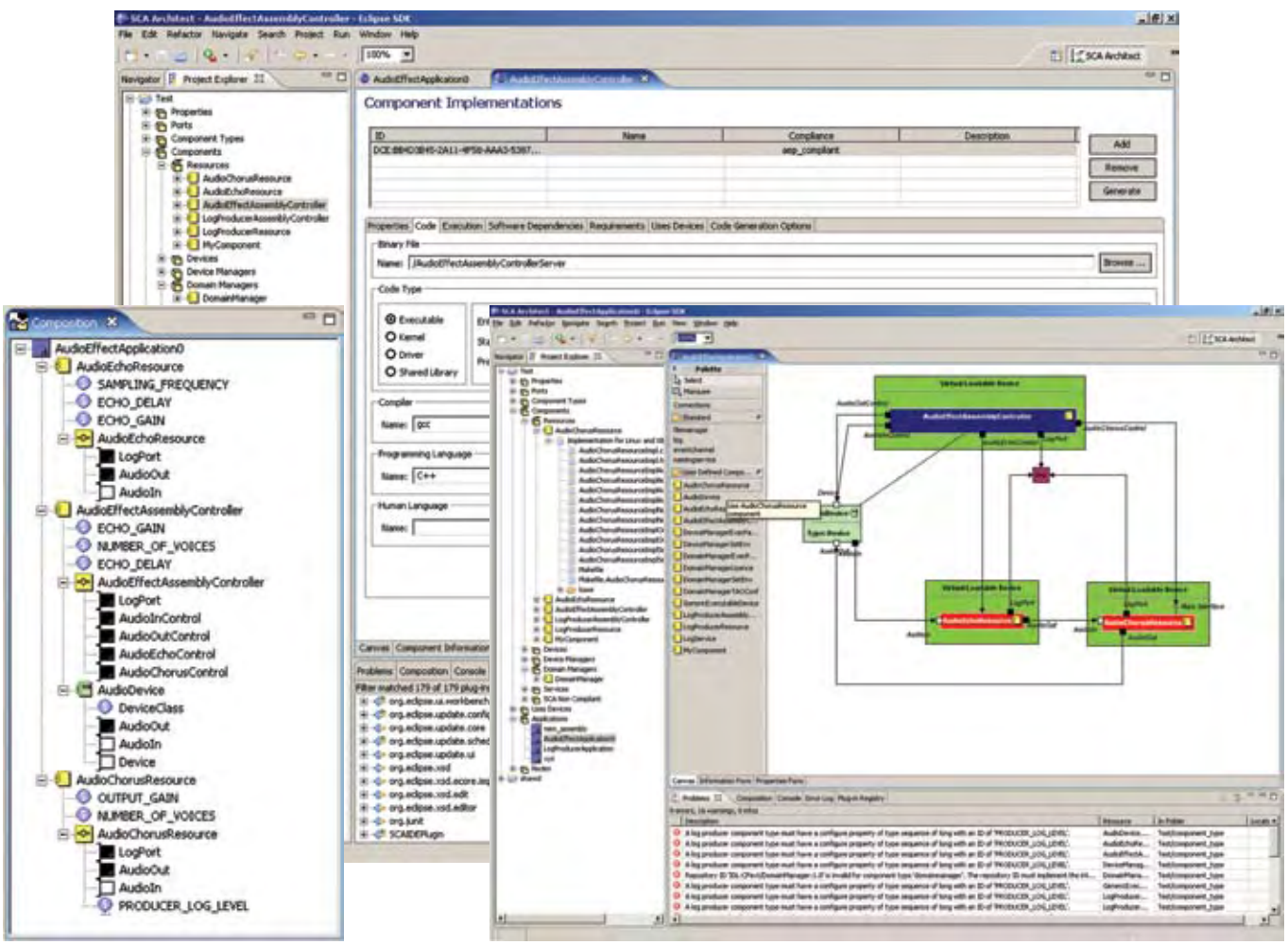


Figure 2

Screen shots of the SCA Architect, a component of CRC's SCARI Software Suite. The Suite enables the development of SCA applications and platforms.


Figure 3

The SCA holds the potential to play a role in countless applications in our daily lives, from public security to consumer electronics.

different jurisdictions often need to operate in coalition. Just like military organizations, communications interoperability is an essential element of the operation. For public safety, however, the cost of radios is often an even bigger challenge. Adopting standard development practices, supported by off-the-shelf products, could provide a solution to lowering manufacturing costs and offer greater flexibility to the end user.

On the commercial front, a significant effort is currently being made to standardize the base station architecture, in an attempt to lower development and deployment costs. The Open Base Station Architecture Initiative (OBSAI) and the PCI Industrial Computer Manufacturers Group (PICMG) are two of the main organizations working toward defining industrial specifications for the signal processing platforms and hardware interfaces. Coupled with the AdvancedTCA architecture and hardware interfaces, the SCA could offer a complete development environment enabling interoperability of both hardware and software, thus minimizing costs even further.

The specification for the SCA core framework does not tie the development of applications to radios. What specifies the domain of applications is found in Annexes of the specification, in the Application Programming Interfaces (APIs) or in the Security supplements. The former identifies interfaces common to radios while the latter limits the domain to military radios. Replacing or adapting these two Annexes could open the door to many new markets for the SCA industry. For example, instead of controlling frequency generators, power amplifiers and antenna gimbals, the software could control pressure, oil and speed sensors, fuel control emissions and entertainment devices, then be used in the automobile industry. Likewise, if the software is related to cockpit controls and flight operations, then it becomes relevant for the avionics industry.

In the realm of modern electronic test equipment, such as oscilloscopes, spectrum and network analyzers, digital signal processing techniques are used extensively to analyze and represent the input signals. Here, the development of software by components would again facilitate commonality of the signal processing platforms, enabling one unit to perform multiple functions (Figure 3).

With the development of faster and more power-efficient signal processors, software will continue to expand its control over our electronic equipment to a point where it will undoubtedly represent the larger cost of the unit. Component-based development approaches are being used to minimize the development cost by creating reusable software components that can be assembled to create applications. Going one step further, by enabling the components to operate on multiple hardware platforms or be isolated from hardware upgrades, additional cost savings could be obtained in the long run.

The SCA has been designed to offer a platform-agnostic environment that can address many of today's software development challenges. From the signal processing platform vendors to the SCA framework and its associated development tools, a complete industry has now been developed to support commercial off-the-shelf products. The future of SCA promises to even further simplify application development and reduce development costs, which is a winning proposition all around. ▮▮

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# Special Feature

Software Defined Radio

# The Power of Software Defined Radio: A Holistic Approach to Designing SDRs for Power

Traditionally, the focus has been on reducing the power consumption of SDR hardware, but it's clear that software also has a major impact, so a holistic approach to reducing SDR power is required. A testbed that can function as an SDR can go a long way in taking the guesswork out of this problem.

Manuel Uhm, Senior Marketing Manager
DSP Division, Xilinx

Software defined radio (SDR) is already a proven reality, thanks to programs such as the U.S. Joint Tactical Radio System (JTRS). However, there are many issues that severely limit the widespread deployment of SDRs, not the least of which is power.

Power is a major consideration in the design of every subsystem of an SDR, especially since they tend to consume more power than hardware radios. As an example, the radio frequency (RF) front end must have sufficient transmit power for the radio's intended range, typically in the order of 5-10 km, depending on the link. Also, for radios running on batteries, the power consumption of the RF front end, modem and the crypto processing subsystems directly impacts the operational lifetime of the radio. In addition, the ability to dissipate the heat generated by the modem has a direct impact on the radio lifetime, and even potentially on the number of channels that can be processed concurrently in a chassis. And there is more.

Hence, reducing the power of an SDR has numerous benefits that can even include reduced operational expenses from having to purchase fewer spare batteries. Here, the focus will be on a holistic approach to reducing the power consumption of the modem of an SDR in order to capture some of those benefits.

## The Hardware Approach to Reducing Power

The first place most people look to reduce power consumption in the modem is in the processing hardware, which is typically comprised of a field-programmable gate array (FPGA), digital signal processor (DSP) and general-purpose processor (GPP). It is important to distinguish between two sources of power consumption in any hardware device—static and dynamic. Static power consumption is the inherent power consumed by a device that is on but not active, and it is dominated by the current leakage of the transistors. Dynamic power, on the other hand, is the power consumed by active usage of the device, which is affected by a number of variables including supply voltages, number of accesses to external memory, data bandwidth, etc. It is important to monitor both types of power consumption, particularly in the case of a radio that has a duty cycle that typically involves more receiving than

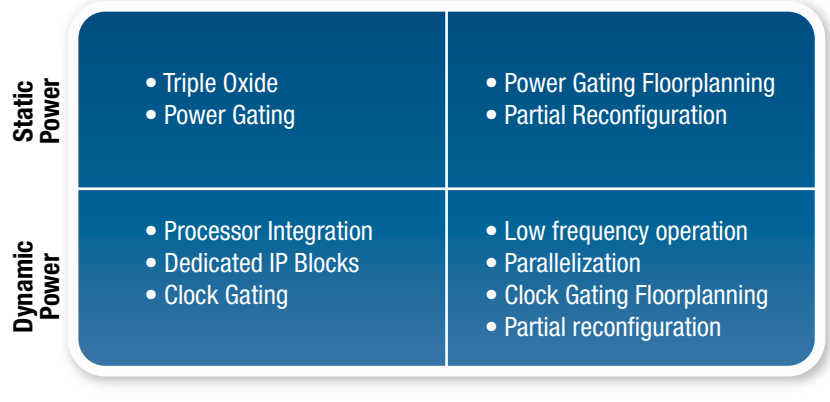


Figure 1

A holistic approach to reducing power in SDRs would ideally use multiple techniques from each quadrant.

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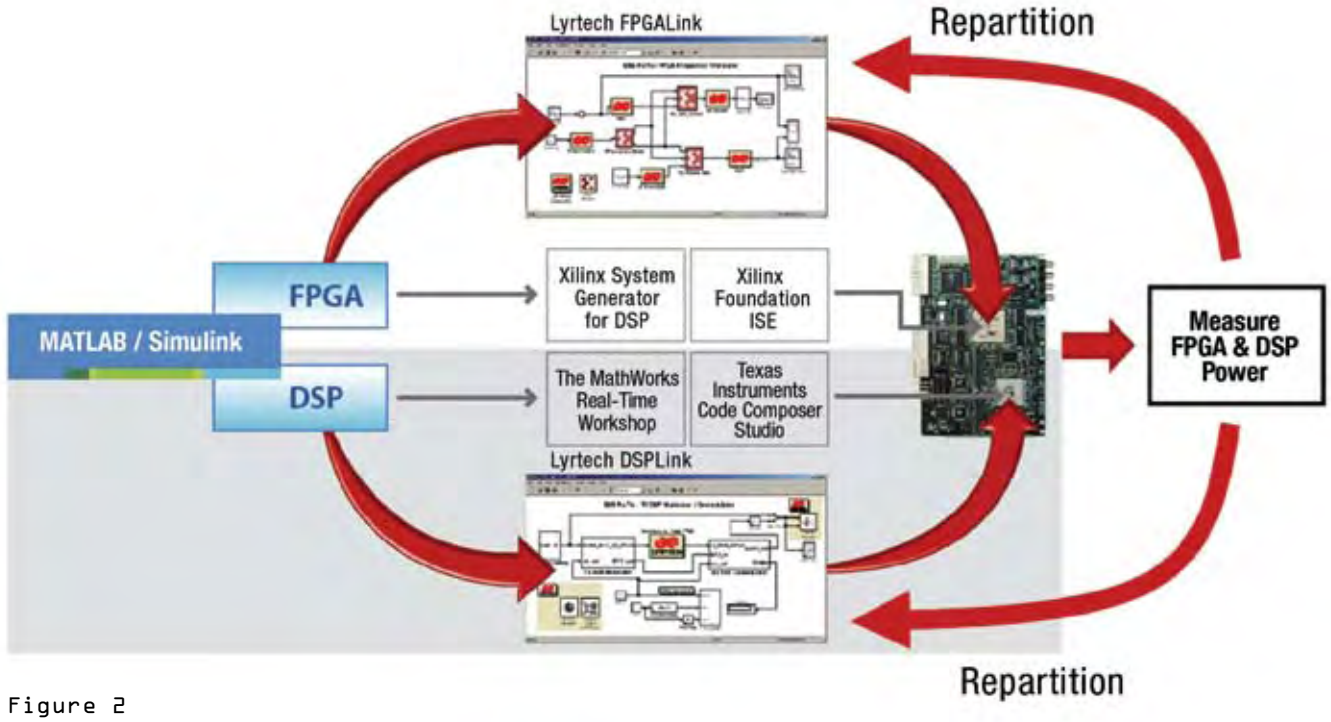


Figure 2

Model-based design flow with power measurements can simplify waveform partitioning decisions.

*(Diagram courtesy of Lyrtech)*

transmitting. In the case of GPPs and even DSPs, power management features such as frequency scaling, voltage scaling and power down modes have become increasingly common. But, what about FPGAs?

There are numerous methods that can be used to reduce static or dynamic power consumption in an FPGA, many of which are not mutually exclusive. Some methods of reducing static power consumption include *triple oxide* and *power gating*.

With *triple oxide*, silicon vendors coat transistors with an oxide to reduce leakage—the thicker the coating, the less leakage. The trade-off is performance. It has been common to use thin oxide in the core where performance is required, and use thick oxide for the I/Os to drive higher voltages. The addition of a medium oxide can significantly reduce leakage where maximum performance is not required, such as configuration SRAMs. Examples of FPGAs taking advantage of this technology include the Xilinx Virtex-4 and Virtex-5 families.

*Power gating* involves the usage of transistors to reduce standby leakage when an FPGA block is not being utilized. An example of this technique can be seen in low-power sleep modes. For example, if all the blocks in an FPGA are power gated, the device consumes very little static power. The trade-off, in this case, is a loss of the configuration of the FPGA such that the device has to be completely reconfigured during the wake-up process, which can take milliseconds. On the other hand, if all blocks are power gated except those with configurations (i.e., configuration memories), then the state of the FPGA is retained. Although the wake-up time is significantly decreased, the power saving is not as significant as when all blocks are power gated. The Xilinx Spartan-3A family of FPGAs supports both types of power gating.

Dynamic power consumption is the other part of the power equation. Methods of reducing dynamic power consumption include *processor integration*, *dedicated IP blocks* and *clock gating*.

*Processor integration* is a classic value proposition for platform FPGAs with embedded GPPs and DSP engines. By using an embedded GPP, rather than a discrete GPP, power savings are derived by not having to drive data from the FPGA to the GPP across external I/O lines, which can typically consume a significant amount of power. Virtex-4 FX devices are an example of a platform FPGA.

Having *dedicated IP blocks* to perform certain common functions can significantly reduce dynamic power without a major impact on flexibility. An example is having a dedicated DSP engine in an FPGA to perform multiply-accumulates. This dedicated IP block can perform that function at much higher performance and up to 85% lower power than logic. The Virtex-5 devices have many dedicated blocks including DSP engines, Ethernet MACs and PCI Express endpoints to provide advanced functionality at lower power.

The *clock gating* technique uses circuitry to disable clocks of FPGA blocks that are not in use, thereby reducing the power consumption in that block to the amount of leakage current. FPGAs such as Virtex-4 and Virtex-5 devices support this capability.

Since it is important to reduce both static and dynamic power, the most powerful approaches to lowering power from

a hardware perspective impact both. One of the best examples is lowering the core voltage. Processing devices tend to benefit from lower voltages as they move to the next process node (i.e., from 90 to 65 nanometers). As an example, the core voltage of a 65 nm Virtex-5 FPGA is 1.0V, 17% lower than the 90 nm Virtex-4 FPGA at 1.2V and 33% lower than the 130 nm Virtex-II FPGA at 1.5V. This is one benefit to using the most current devices. Lower core voltage has a significant impact on both static and dynamic power, since leakage scales exponentially with voltage and dynamic power scales quadratically. As a result, Virtex-5 devices average over 30% lower static and dynamic power than Virtex-4 FPGAs.

The discussion has covered several hardware approaches to reducing power consumption in an SDR, which is great—but it feels like something is missing. After all, isn't this called SOFTWARE defined radio? Although designers like to talk to hardware providers about reducing the power consumption of their devices, the reality is that many so-called "hardware companies" have more software engineers than hardware engineers. Surely, this would seem to indicate that there is more to power consumption than just hardware.

## A More Holistic Approach to Reducing Power

Well, there certainly is, and to truly optimize SDRs for power consumption one needs to take a more holistic approach, combining both hardware and programming techniques. An inefficiently implemented waveform can have a tremendous negative impact on an SDR's power consumption regardless of how well the hardware is designed. There are many techniques that one can use to implement a waveform more efficiently in an FPGA, including *parallelizing the algorithm*, *low frequency operation*, *floorplanning for power* and *partial reconfiguration*.

With *parallelizing the algorithm*, it is well documented that the parallelism offered by FPGAs allows for much higher performance signal processing than is possible from sequential processors such as DSPs or GPPs. Since parallel processing can perform tasks at much lower clock frequencies than required by sequential processors, FPGAs can actually be more energy efficient than processors when parallelizing the algorithm.

With *low frequency operation*, many military waveforms can benefit from running at lower frequency to reduce power consumption. It is common for waveforms to be running in an FPGA at less than 200 MHz, well below the maximum frequency.

Some of the techniques described above, such as clock gating, can be much more effective with some careful *floorplanning* of the design. For example, to truly take advantage of clock gating, one would want the portions of a design utilizing the same clock that could be gated located in the same area, perhaps in a quadrant of the device. Commercially available tools such as the Xilinx PlanAhead design and analysis tool significantly ease floorplanning with a graphical user interface (GUI).

*Partial reconfiguration* (PR) allows a designer to time multiplex the resources within an FPGA. Without PR, one would have to reload the entire FPGA to support a new waveform mode, thereby temporarily losing the comms link, or have all modes loaded concurrently in a large FPGA even though only one mode is being used at a time. PR allows support for multi-mode waveforms without having all the modes loaded into the FPGA concurrently, thus enabling the same functionality with a smaller, lower power FPGA. Efficiently using PR also benefits from floorplanning. Similar to low core voltage, PR can impact both static and dynamic power, whereas the techniques above only affect dynamic power.

Figure 1 illustrates these various approaches to reducing power. A truly holistic approach to reducing the power of SDRs would use multiple techniques from each quadrant.

Given the numerous approaches to reducing power in an SDR, many of which can be combined, it would seem that there could be little chance to determine the ideal power-optimized waveform implementation. Add to the mix that many waveform components like Forward Error Correction (FEC) can often be efficiently implemented in either an FPGA or DSP. It is often not clear how best to partition a waveform between hardware and software to maximize energy efficiency. While there is no magic bullet—no tool that can assess all the various options and permutations to definitively identify the optimal solution—there must be a better way than sheer guesswork by using published datasheet numbers and spreadsheet-based power estimators.

## Taking out the Guesswork: The SDR Power Optimization Testbed

A far superior approach would be to have access to an SDR that could serve as a

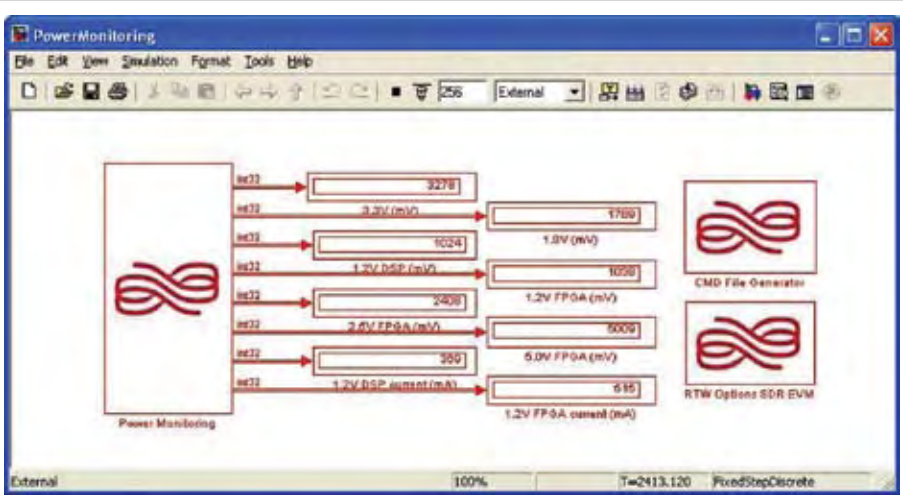


Figure 3

A Power Monitoring GUI displays power consumption of the modem FPGA and DSP to take the guesswork out of developing waveforms for power.

*(Diagram courtesy of Lyrtech)*

testbed for power-optimized designs. Having such a testbed would allow a designer or system architect to empirically test and weigh the trade-offs associated with a specific hardware and software design for power. The designer could not only compare the relative merits of some of the techniques discussed above, but could also iteratively develop and partition a waveform between an FPGA and DSP/GPP with relative ease, while taking power measurements on each modem processing device.

Although not necessary, using the concepts of model-based design can also provide benefits by easing the waveform repartitioning via modeling in a visual manner. An example of such a design flow can be seen in Figure 2. In this example, a waveform can be modeled using Simulink from The MathWorks. The designer can choose to partition the waveform between an available FPGA and DSP and go directly to implementation on the hardware using the Xilinx System Generator for DSP and ISE Foundation design suites for the FPGA, and The MathWorks Real-Time Workshop and Texas Instruments Code Composer Studio for the DSP.

The designer can also use a Power Monitoring GUI from within the model-based design environment to display real-time power measurements being logged for the FPGA and DSP independently. An example of such a GUI can be seen in Figure 3. This logging capability allows the designer to make educated decisions about the energy efficiency of the waveform over time, not just a snapshot in time. This is necessary since many waveforms are "bursty" in nature. Should it become apparent that the waveform implementation causes the modem to exceed its power budget, the designer can go back to the model and repartition the waveform for better efficiency. Although this flow is not "push button" today, it is worth the effort as it does remove the guesswork out of estimating the power consumption of the modem.

Such an SDR testbed with power monitoring is available today through the collaboration between Xilinx, Texas Instruments and Lyrtech. The Small Form Factor SDR Development Platform combines a Virtex-4 FPGA with a DM6446 DSP/GPP to empower designing for low power.

## Designing for Power

Although traditionally the focus has been on reducing the power consumption of the SDR hardware, it is clear that software also has a major impact on power consumption. As such, a holistic approach to reducing the power of SDRs is required. Furthermore, a testbed that can actually function as an SDR can go a long way in taking the guesswork out of this problem. Although this approach can take more planning and development effort up front, the benefits are compelling and empower SDR providers with a competitive advantage in supplying radios that last longer in the field, are more reliable and require fewer spare batteries. ■■

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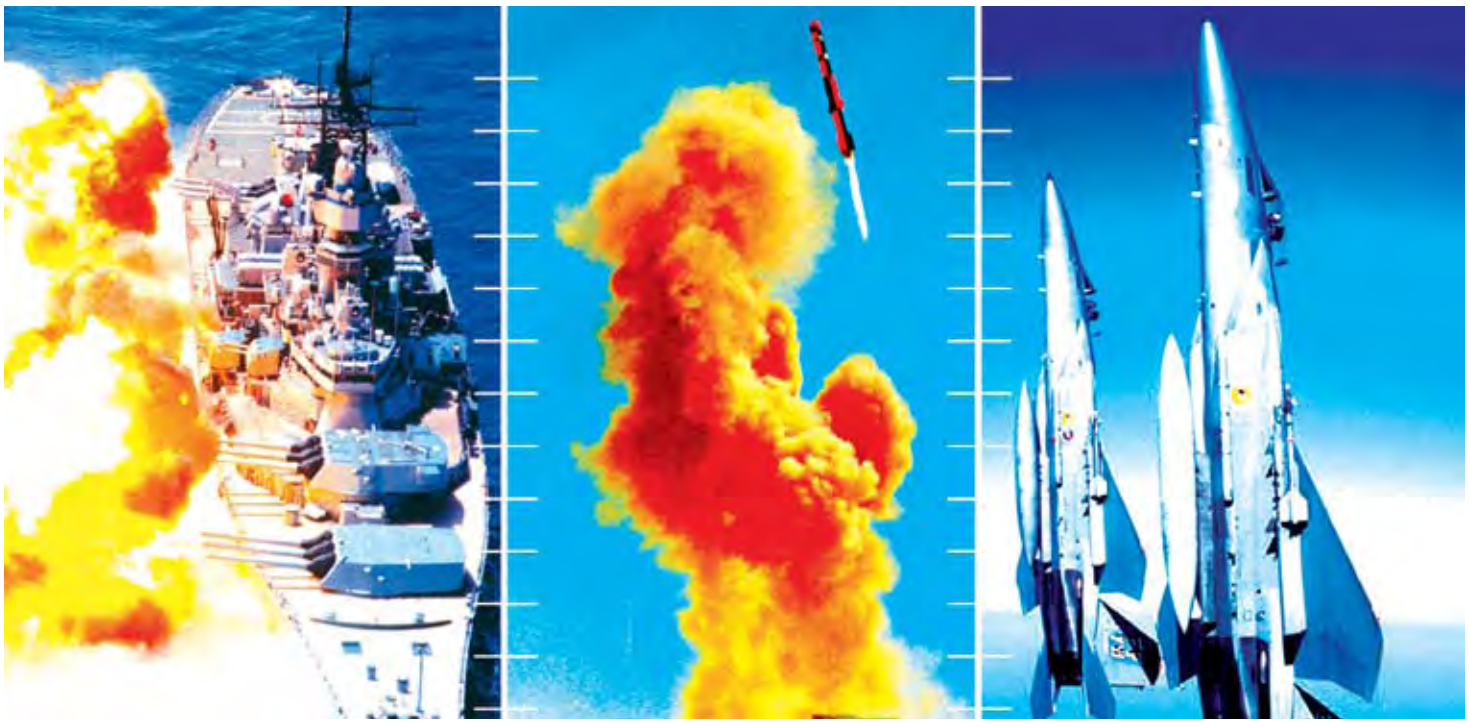

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# CORBA for FPGA: The Missing Link for SCA Radios

Enabling CORBA on DSPs and FPGAs for SDR provides a variety of advantages for the builders of software defined radios.

Joe Jacob, Senior V.P. Sales & Marketing
Objective Interface Systems
Maxime Dumas, Field Applications Engineer
Lyrtech

As the first generation of software defined radios built for compliance with the U.S. Military's Joint Tactical Radio System Software Communications Architecture become available for deployment, radio manufacturers continue to innovate to create ever more powerful radios in smaller and smaller form-factors. In order to drive down costs, they continue to increase their use of off-the-shelf tools. Their goal is to reduce development and deployment costs while enabling more flexible design options throughout the engineering process.

As radio builders research and develop new prototype radios, they discover they can never have too much processing power. As waveforms become larger and more complex, many radio builders are running into a performance wall as they try to manage multiple large waveforms at the same time. Modern software defined radios (SDRs) often use a combination of general-purpose processors (GPPs), digital signal processors (DSPs) and field programmable gate arrays (FPGAs) to provide the processing power necessary to build SDRs that meet their extensive engineering requirements.

Existing versions of the Software Communications Architecture (SCA)—including the most recent edition, version 2.2.2—provide component flexibility for the GPP. One of the issues for the current publicly available standard is that it does not specify equivalent component flexibility for the DSPs and FPGAs. Recently, the JTRS Joint Program Executive Office has specified the Modem HW Abstraction Layer (M-HAL) as a mechanism for providing some of that component flexibility.

However, M-HAL is not a solution for the general market. Under ITARS (International Traffic in Arms Regulations), its distribution is restricted and thus the details of the technology are not available to the general public or to the international community of radio builders. It is also not a COTS solution, so it cannot take advantage of the reduced costs and ubiquity and breadth of application that a COTS product provides.

## The Breakthrough

Software vendors have responded by providing high-performance off-the-shelf technologies to increase performance and

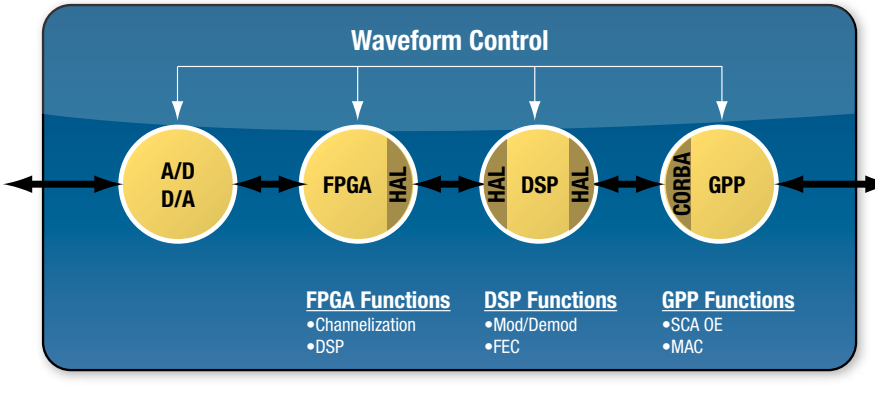


Figure 1

The architecture of current SCA-compliant radios.


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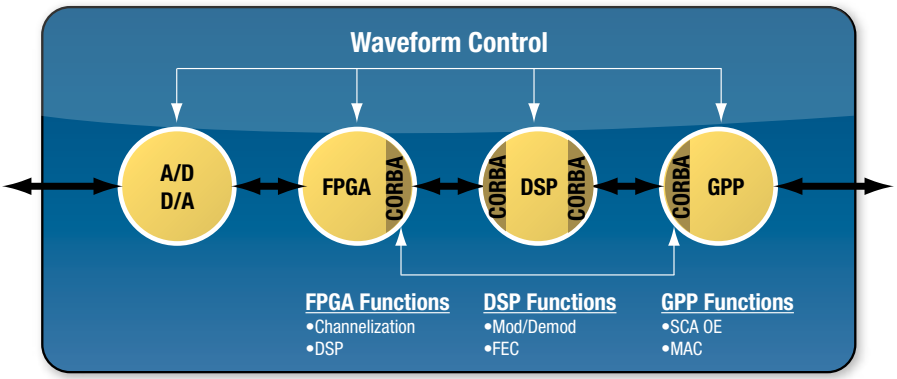


Figure 2

The architecture of next-generation, all-CORBA, SCA-compliant radios.

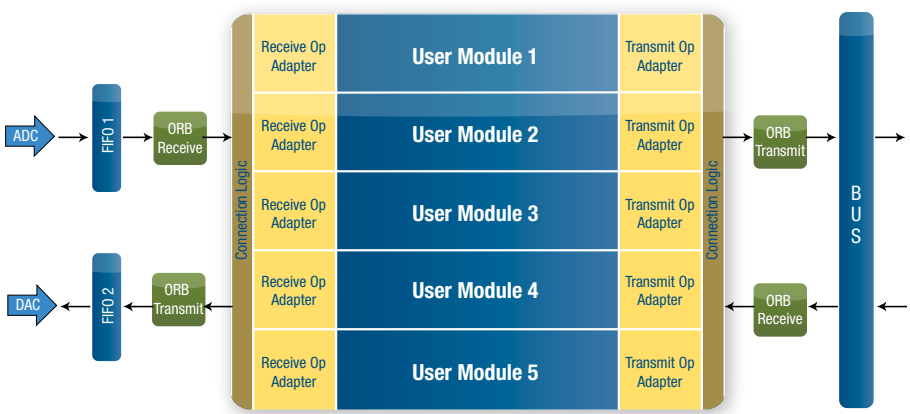


Figure 3

Floorplan of the CORBA solution for FPGA.

provide broad, wide-ranging component flexibility for radios across a variety of different hardware devices. An important part of these new technologies is providing a standards-based CORBA implementation for specialized processors. For the past few years, ORBs have been available for most DSPs, but up until very recently FPGAs were left out. Building an ORB for FPGA implies several challenges, mainly due to the fact that programming is still done at a very low level, and that designs are tightly linked to specific resources of the programmable fabric—for FPGAs, there is no equivalent to the virtual addressing provided by operating systems. In spite of this, enough functionality can be attributed to the FPGA in order for it to be recognized as an SCA device. In fact, because of the parallel processing nature of configurable logic devices, the greatest advantage of an FPGA ORB is its performance, as it does not need to preempt the processor for a context change.

Objective Interface Systems designed a CORBA solution for FPGAs that creates an abstraction layer between the developer's modules (components of a waveform) and the hardware communications interfaces. This solution, implemented in the Lyrtech Small Form Factor SDR Kit, allows the FPGA to be loaded with several components. What puts this solution at the state-of-the-art for component-based development is that it exploits the full potential of the partial reconfiguration feature of the Xilinx chips. By constraining the design of the various components to predefined areas of the FPGA at development time, it gives the possibility to instantiate partial bitstreams and individually load multiple resources onto the FPGA at run-time, acting more like an executable device, as opposed to a loadable device.

Allowing developers to do this gives flexibility on the granularity of the components to be created and is in line with one of the goals of the SCA—to develop and deploy waveform components distributed across multiple processors without any initial knowledge regarding where other components are located, whether they reside on the same processor, or on different ones. This does not mean that it has not been tailored for performance. In fact, one of the key features of the FPGA ORB is that communications between two components that reside within the same FPGA are simplified so as to minimize the latency as well as the overhead in logic. A sophisticated but lightweight connection infrastructure routes these internal messages directly to the appropriate FPGA component, while messages for CORBA objects that exist external to the FPGA are transparently routed to the ORB for full GIOP (General Inter-ORB Protocol) processing

Figures 1 and 2 illustrate respectively the architecture of current radios, based on SCA 2.2.2, and the architecture of the next generation of radios, implementing CORBA across all processors. Figure 3 presents a detailed floorplan of how the CORBA solution for FPGA is laid out. In this particular case, the FPGA resides between a DSP and the A/D and D/A converters. For illustration purposes, parts of a spread spectrum waveform have been added in the figure.

## Design Flow

Although the design of the FPGA ORB is very different from the design of traditional ORBs, the design flow a developer needs to follow is somewhat similar. Starting with the source code, a developer

first needs to define the interface definition language (IDL) for a given component. Using the IDL-to-VHDL translator, some adapter code is generated, which has to be linked to the waveform component. Specifying pre-defined location constraints to the module and following the partial reconfiguration design flow will result in a partial bitstream that contains everything it needs to communicate with the ORB and/or with other components and allows it to be dynamically loaded at any time. If a component requires more FPGA resources than a single placeholder offers, the developer can constrain its design to a larger area. Figure 4 shows the floorplan of a Virtex-4 SX35 containing the ORB (in pink), the transport adapters (in yellow and green), the usual I/O interfaces and glue logic (in dark red and blue), and a single SCA resource (in dark green).

In order to make the FPGA ORB an off-the-shelf solution, its design needs to be platform-agnostic as much as possible. In fact, its only dependency is on the number of ORB instantiations, which depends on the number of different physical transports the FPGA will use to communicate with other CORBA-enabled devices.

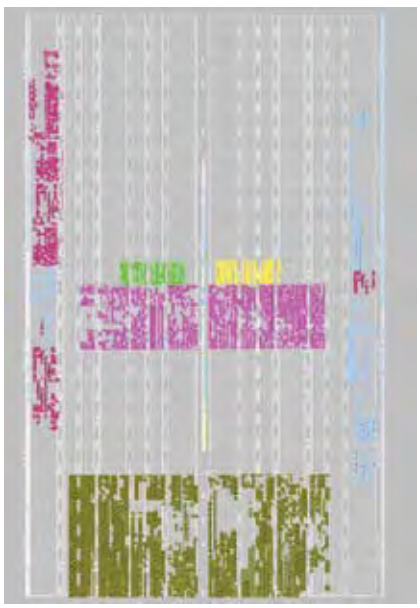

Figure 4

The place and route result of a waveform component and the FPGA ORB. This is the floorplan of a Virtex-4 SX35 containing the ORB (in pink), the transport adapters (in yellow and green), the usual I/O interfaces and glue logic (in dark red and blue), and a single SCA resource (in dark green).

## The Platform

The FPGA ORB has been integrated into Lyrtech's Small Form Factor SCA Development Platform (SFF SCA DP), the first development platform to include a CORBA-enabled FPGA. The complete software tools integration allows developers to readily create SCA components using standard, non-restricted, hardware-agnostic communication interfaces for GPP, DSP and FPGA processors. In this way, the partitioning of the waveform on the processors can be revisited at any time during development or after deployment without modifying the structure of the application; only the platform-specific implementation of the migrated CORBA operations need be considered.

Enabling CORBA on DSPs and FPGAs for SDR provides a variety of advantages for radio builders. In many development shops, the GPP, DSP and FPGA development groups work in isolation. ORB-enabled GPPs, DSPs and FPGAs provide a common communication description between disparate engineering disciplines. As the SCA is already based on CORBA, it extends the robust technology throughout the radio, preserving SCA compliance while increasing portability of algorithms and logic. Systems engineers can now move functionality to FPGAs *without* modifying the structure of their applications.

The system architect can migrate functionality from GPP to FPGA as needed. Assignment of functionality does not need to be decided early in the radio development process. Functionality can be tested on GPP, and then migrated to FPGA as needed, without changing the main application. For the first time, entire unified radio designs can be done on a workstation and then piece-by-piece moved to the relevant processing device.

Specialized interfaces for DSPs and FPGAs are no longer needed. System architects can maintain their focus on improving functionality in the radio while the ORBs provide the necessary interface details for the GPP, DSP and FPGA code developers. For the first time, full technology transparency is feasible in heterogeneous system architecture for SDRs. The technology is available today and has no ITARS restrictions, so development teams can use it worldwide.

A number of different SCA-based SDR programs around the world are prototyping systems with ORBs for all devices in the radio, including DSPs and FPGAs. In doing so, they are reaping the benefits of high performance, low power and small footprint requirements through the use of this standards-based architecture. ▮▮

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# Tech Recon

Military Market Update

# Budgets, Politics and Industry Shifts Roil Military Embedded Computers/Electronics Market

The military market remains tentative as the political environment keeps pundits guessing about the military budget, the war in Iraq, the future of many programs and the overall direction of the economy. The embedded electronics portion of that market has struggled in 2006, and 2007 looks only slightly better.

Warren Andrews
Editorial Director

The past year has been one of frustration for a variety of vendors looking to complete projects started months and even years ago. And the future remains questionable as many programs are being reduced, or in some cases, eliminated. The highly touted Future Combat Systems (FCS), (the military's second largest behind the $276 billion F-35 Joint Strike Fighter) for example, will be clipped some $3.3 billion in the short run deferring four projects and delaying production.

Other projects will undoubtedly face similar fates as the Pentagon continues to rein in costs. The Army is looking to save another $4.1 billion by terminating 11 systems. All these proposed savings are said to be needed to pay for the war in Iraq, cover higher recruiting and retention costs, repairing badly damaged hardware assets and mobilize the National Guard and Reserves.

Figure 1

The F-35 Lightning II Joint Strike Fighter made its initial flight Dec. 15. The new fighter is the most expensive program in the military's lineup costing some $276 billion. The Air Force is looking to include at least three of these new aircraft into its emergency supplemental funding this year to replace damaged, lost and aging F-15s and F-16s.

*(Lockheed Martin photo/David Drais).*

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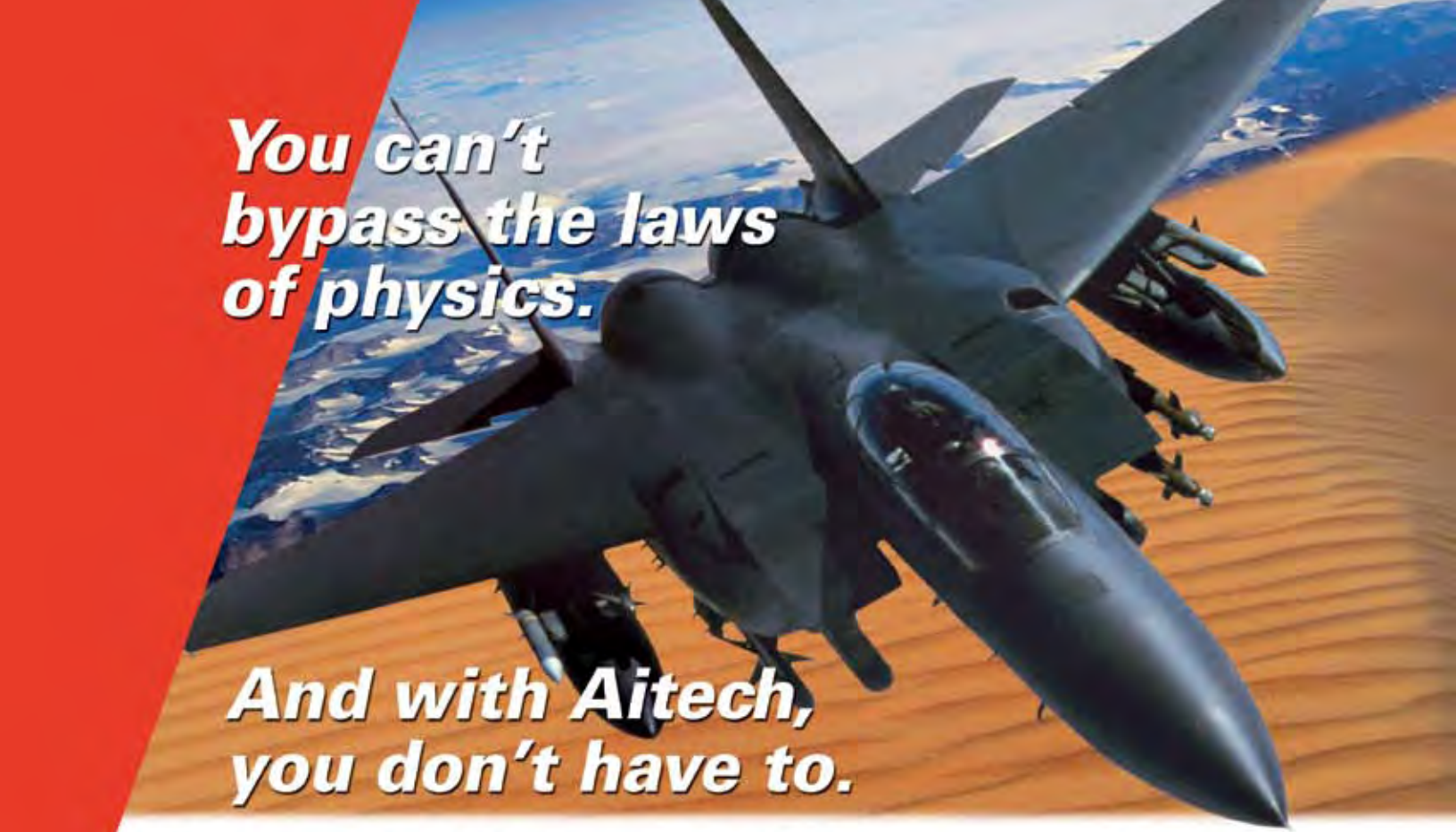


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| Bus | AT Expansion Bus | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | PCI Universal Expansion Bus | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | |
| | PCI Bus Masters | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | | 4 | 4 | | |
| | APIC (add'l PCI interrupts) | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | |
| CPU and BIOS | CPU Max Clock Rate (MHz) | 1400 | 1400 | 1400 | 1400 | 650 | 650 | 650 | 650 | 650 | 650 | 333 | 333 | 333 | 100 | 100 |
| | L2 Cache | 2MB | 2MB | 2MB | 2MB | 256k | 256k | 256k | 256k | 256k | 256k | 16K | 16k | 16k | 16k | 16k |
| | Intel SpeedStep Technology | ✓ | ✓ | ✓ | ✓ | | | | | | | | | | | |
| | ACPI Power Mgmt | 2.0 | 2.0 | 2.0 | 2.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | | | | | |
| | Max Onboard DRAM (MB) | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 256 | 256 | 256 | 32 | 32 |
| | RTD Enhanced Flash BIOS | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Nonvolatile Configuration | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Quick Boot Option Installed | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | USB Boot | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | |
| Peripherals | Watchdog Timer & RTC | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
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| | SSD Socket, 32 DIP | | | | | | 1 | | 1 | | 1 | 1 | 1 | | 2 | 1 |
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| | Audio | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | |
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| | Analog Video | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | SVGA | | |
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| | PS/2 Mouse | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
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| | USB 2.0 Ports | 2 | 4 | 2 | 4 | | | | | | | | | | | |
| | USB Ports | | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | | |
| | 10/100Base-T Ethernet | 1 | | 1 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| | ECP Parallel Port | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | aDIO(Advanced Digital I/O) | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | | |
| | multiPort(aDIO, ECP, FDC) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| SW | ROM-DOS Installed | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
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| | Data Marker Inputs | 3 | 3 | | 3 | | 3 | | | | | | | | |
| Conversions | Channel-Gain Table | 8k | 8k | | 8k | 8k | 8k | | | | | | | | |
| | Scan/Burst/Multi-Burst | ✓ | ✓ | | ✓ | ✓ | ✓ | | | | | | | | |
| | A/D FIFO Buffer | 8k | 8k | | 8k | 8k | 8k | | | | | | | | |
| | Sample Counter | ✓ | ✓ | | ✓ | ✓ | ✓ | | | | | | | | |
| | DMA or PCI Bus Master | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | | | | | | ✓ | |
| | SyncBus | ✓ | ✓ | | | | ✓ | | | | | | | | |
| Digital I/O | Total Digital I/O | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 48 | 18/9 | 32 | 64 | 32 | 48 | 48 |
| | Bit Programmable I/O | 8 | 8 | | 8 | 8 | 8 | 8 | 24 | 6/0 | | | | 48 | ✓‡ |
| | Advanced Interrupts | 2 | 2 | | 2 | 2 | 2 | 2 | 2 | | | | | 2 | |
| | Input FIFO Buffer | 8k | 8k | | 8k | 8k | 8k | | | | | | | 4M | 8M |
| | Opto-Isolated Inputs | | | | | | | | | | 16 | 48 | 16 | | |
| | Opto-Isolated Outputs | | | | | | | | | | 16 | 16 | | | |
| | User Timer/Counters | 3 | 3 | 3 | 2 | 3 | 3 | 3 | 3 | 3 | | | | 10 | 6 |
| | External Trigger | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | ✓ | |
| | Incr. Encoder/PWM | | | | | | | | | 3/9 | | | | | ✓‡ |
| | Relay Outputs | | | | | | | | | | | | 16 | | |
| Analog Out | Analog Outputs | 2 | 2 | | 2 | 2 | 2 | 4 | | | | | | | |
| | Max Throughput (kHz) | 200 | 200 | | 200 | 100 | 200 | 200 | | | | | | | |
| | Resolution (bits) | 12 | 12 | | 12 | 16 | 12 | 12 | | | | | | | |
| | Output Ranges | 4 | 4 | | 3 | 1 | 4 | 4 | | | | | | | |
| | D/A FIFO Buffer | 8k | 8k | | | | 8k | 8k | | | | | | | |

‡ User-defined, realizable in FPGA

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As new programs are paired back, older equipment is being upgraded and technology insertion is critical.

Similar cuts are expected across the other services as major sea and air programs are continually being evaluated and modified. On one hand, cuts in new and emerging programs have not always been bad for the embedded computer and electronics industry. As new programs are paired back, older equipment is being upgraded and technology insertion is critical. That's the good news. On the other hand, when these cuts go too deep, and when funds from major programs have to be sidetracked to keep the wheels of the current deployed forces oiled, everything suffers—including upgrades and technology insertion.

But lest one be too pessimistic, there is some good news in the offing. Analysts believe the DoD will ask for an additional $100 to $130 billion in supplemental funding. Let's now add that to the $70 billion in bridge funding already approved and pile that atop the budget of $462.8 billion, and the total defense spending could reach over $660 billion.

The recent trend has been for supplements to be approved by Congress with little resistance. However, with the new Congress, the supplemental budget may be scrutinized a little more carefully. In the recent years, the DoD tended to include lots of things in supplemental budgets that in the past may have been in the basic budget. The Air Force, for example, is likely to ask for up to 17 additional C-130J transport planes to replace those lost in combat, training, or just plain worn out. The Air Force is also expected to try and include at least three F-35 (JSF) fighters (Figure 1) to replace aging or lost F-16s and F-15s. So for the embedded market it resembles something like playing musical chairs. Expect existing programs to remain in force—with the same kind of delays experienced this year.

The Army, with the biggest requirements, wants an additional $49 billion in addition to the $44 billion in bridge funds and the $80 billion it proposed back in November. The Marine Corps too wants to replace aging and damaged CH-53 Helicopters with Osprey tiltrotors. And the list goes on.

Further, there continues to be talk about increasing the overall size and scope of the military to better address the type of conflict the nation is seeing in Afghanistan and Iraq and the overall war on terror. President Bush has indicated that this is essential not only for the current conflicts, but to address future needs. As the budget is put together and reviewed by both the OMB and Congress, we'll see what kind of strength the military can muster in terms of increasing its budget.

Even with the emergency supplemental budgets, prime defense contractors are not comfortable. A recent headline in a defense publication proclaimed, "Tighter Pentagon Budget Will Force U.S. Firms to Look Beyond Defense." And while companies such as Lockheed Martin and Boeing are looking outside of the traditional defense markets in order to continue to show the financial results their stock holders have become accustomed to, others such as GE and Raytheon are looking to get more involved in the defense business. For its part, Raytheon is divesting itself of its commercial aircraft business to focus more on its military business. And if GE's recent spate of acquisitions in the embedded computer business for the military (SBS, Condor and Radstone) is any indication, it too wants to strengthen its military posture.

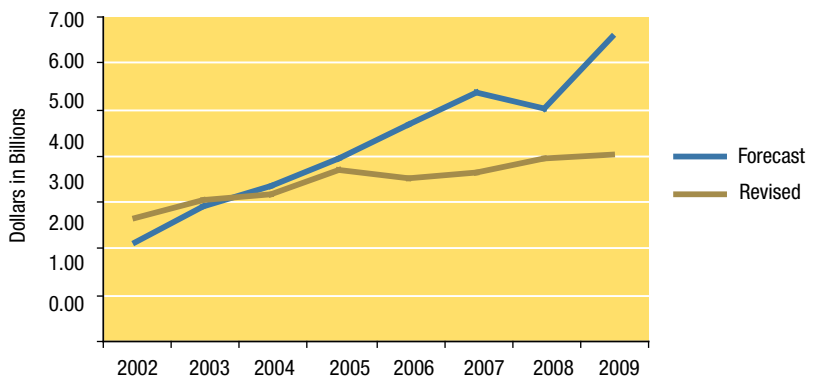


Figure 2

The military market for embedded computers has failed to reach earlier forecasts and is not likely to do so in the immediate future. For 2006, the estimated actual fell almost $1 billion below earlier forecasts. (Dollars in billions.)

## The Embedded Computer Market

The DoD budget numbers are mind-boggling. Back when forecasting the market was relatively easy (which was never), analysts would take a look at the total DoD budget and make some determination of the content of electronics and computers in that total and then further strip that number down to include only embedded computers. Looking at the DoD budget, somewhere in the area of $37 to $38 billion—about 8½%—has been earmarked for computers and electronics. And generally the some 12% to 13% of that number was calculated as the merchant market for embedded computers. Thus, for example, with $440 billion as the budget for 2006—with $37.5 billion of that in electronics and computers—the merchant market for embedded boards, subsystems and systems would represent some $4.5 billion. That didn't happen this year. The total for the merchant market was closer to $3.5 billion.

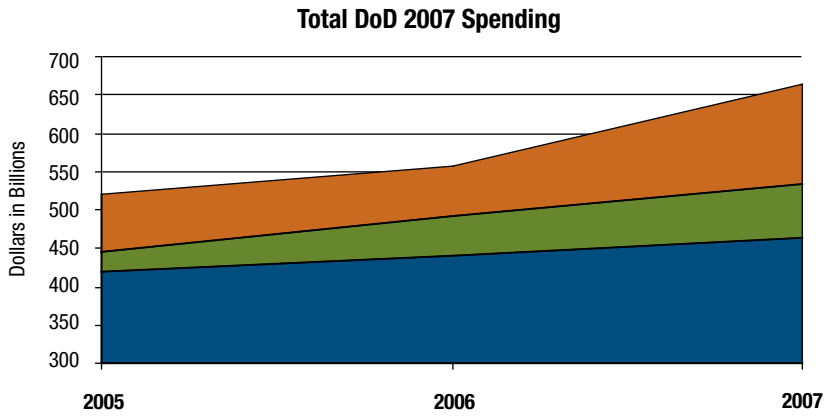


Figure 3

The total defense budget (blue) has been changed by bridge financing (green) and emergency supplemental funding (orange) such that total DoD spending for 2007 is expected to reach close to $660 billion. This is one of the factors that makes forecasting the embedded computer business in the military difficult. (Dollars in billions.)

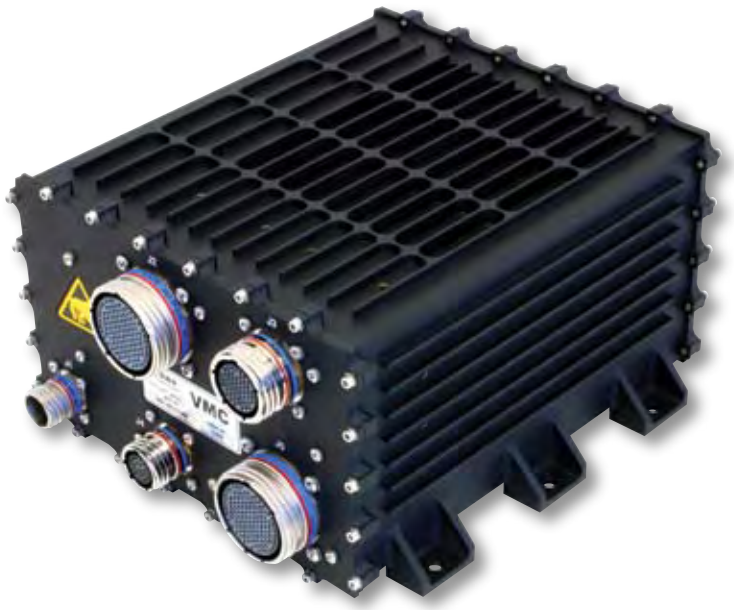

Figure 4

GE Fanuc's AVC-cPCI 3003 is typical of many newer systems that provide a rugged, compact and flexible COTS computing platform for a variety of military applications from UAVs, vetronics and booster vehicles, to commercial aviation. Such 3U cPCI platforms as well as others based on such standards as PC/104, EBX, EPIC, MicroTCA, COMM Express and others, are replacing larger platforms particularly in applications sensitive to size, weight and power dissipation.

What's not clear is the figure for boards and subsystems that never came on the market but were designed and built internally by prime contractors. This figure has always been a crystal ball guess, but government funding policies over the last few years have made it easier for primes to build internally, which may have been a significant factor in not getting closer to the $4.5 billion.

Now it would seem the rules have changed. What, for example, is the total DoD budget? Is 2007 spending $462.8 billion or $660 billion? And if it's the higher number, is the electronics and computers component still 8½%? And, is the old factor of 12% to 13% of that still valid? Based on last year, the answer is that the rules to forecast that number were wrong. Figure 2 shows the figure for the past few years, as close to reality as we can get for this year, showing both our forecasts and what we believe to be the real numbers. We've also added our forecast for the next three years. In years past, we've superimposed these numbers on the DoD budget, but it's getting difficult to know which number to use.

The DoD spending is quite another number from the budget. Looking at the past three years (Figure 3) it's gone from $420 billion to $462.8 billion—an increase of $42.8 billion or a little over 10%. In that same time, bridge funding increased from $25 billion to $70 billion, an increase of $45 billion or 180% increase. And, emergency supplements jumped from $75.9 billion in 2005 to $130 billion in 2007, a staggering $54 billion or over 70%. Many analysts believe that the new Congress isn't going to have the stomach for emergency supplements beyond this year. Therefore, it's likely that either these amounts will have to be added to the main budget—which would swell the budget to over $660 billion—or the DoD will have to dramatically pare down expenses. And many guess that any paring down will be more symbolic than real.

## Technology Concerns

While the battle of the budget continues, technology marches on. Over the past twelve months, new standards—those forged only in the past couple years—have started to take hold. Also, there is more emphasis on system-level products as opposed to boards. In addition, many designs are calling for more compact packaging than in the past, with lower weight and smaller form-factors needed to squeeze into UAVs, small robots, man packs, and other applications where space is limited and weight can be a problem. Whether budgets are increasing or decreasing, the military has always turned to better electronics. The only concern is that when there is ample availability of funds, the money will flow more toward prime contractors and stay with them; when money is tighter there is more flow toward subcontractors.

For example, over the past two years we've seen a number of programs where traditional chassis have been abandoned for complete packages loosely based on 3U CompactPCI (Figure 4). In other areas, we've seen a tremendous increase in PC/104 and its growing number of variants from PC/104+ to EPIC systems being designed in and deployed in a broad cross section of military projects. New and ever efficient packaging, cooling and power solutions will be key to success in greater penetration in the military embedded market.

And, the lonely PC motherboard in variations of its native motherboard form-factor, continues to be a favorite in many applications. From its use in shipboard systems to many of today's advanced simulators as illustrated in the recent Interservice/Industry Training, Simulation and Education Conference (I/ITEC), the latest generation of PC has proven itself worthy. Very much unlike the motherboards of the past, the new generation is rugged, reliable

and ready for battle. If the percentage year-on-year increases of the systems on display are any indication, this form-factor will continue to see double digit growth.

Also, according to some sources, MicroTCA is becoming an unlikely standard to address a variety of communications needs in the military. While the specification was not written to handle the rugged environments encountered in military systems, clever packaging and cooling techniques from such companies as Hybricon, seeing the opportunity to take a leadership position in a new potential market, have begun to solve many of the problems. And, Motorola and a handful of other companies are busy working on a variation of the specification that will address rugged requirements.

What of VME and VITA's cadre of upcoming standards? VME still holds the uncontested crown in the military market for embedded computers. But its margin is gradually eroding as VME starts showing its age. The last of the VME-based standards—those that still maintain the VME bus—is probably VXS. Over the past year we've seen many such systems being deployed and they are starting to step into slots of the conventional VME.

The next-generation standard developed by VITA, VITA 36, completely departs from legacy VME. The VME community continues to have a strong focus on the military market and introduces standards efforts in the VSO to address the future needs of the embedded mil market. There are a few handfuls of systems currently deployed and, according to many, there is a great deal of design-in activity. However, neither VXS nor VITA 36 addresses the requirements for compact, lightweight systems. A current working group for VITA 56 is addressing that need and developing a small form-factor, front-loading, hot-swappable rugged module. Early indications are that it is directly competitive with MicroTCA.

And while VITA 56 will undoubtedly fit a lot of requirements, MicroTCA already has a critical mass of commercial products, and if it can fit a program's requirements, it (MicroTCA) will probably be selected primarily based on price. It seems unlikely at this time that VITA 56 will have a chance to reach the economies of scale that MicroTCA/AMC have already reached.

Finally VITA 58, the foundation of a standard addressing Line Replaceable Units (LRU), began with a flurry of activity and has tapered down somewhat. It's unlikely that this fledgling standard will see any action this year outside of perhaps a few experimental products designed and made by prime contractors and addressing very specific needs.

As we look at the year ahead, the crystal ball is very fuzzy. VME and VXS will continue at roughly the rates of the past two years. VITA 36 is expected to see some deployment this year, however, at the expense of older VME hardware. What, if any, gains we see this year will be in compact, lightweight and low-power systems aimed at newer mobile military systems. And, repackaged motherboards, both standards-based and stand-alone such as General MicroSystems palm-sized PC, will be in increasing demand to service the growing number of portable and mobile systems. ▮▮

# Digital IRIG 106 Enhancement Untaps Potential of Flight Data Recording

The adoption of IRIG 106 Chapter 10, the Digital On-Board Recorder Standard, is sparking a revolution in the way airborne telemetry data is captured, recorded, analyzed and distributed.

Richard Bond, Chief Operations Officer
Heim Data Systems

As network-centric operations continue to revamp the way the U.S Military shares information, high-speeding, high-density data recording is becoming a critical technology. The shift from analog to digital recording technology has the potential to greatly enhance the accuracy and manageability of flight data recording while significantly lowering the cost. Until recently, however, users have not been able to fully realize the benefits of digital technology because of the absence of a widely accepted standard.

During the first generation of digital recording products, individual manufacturers developed their own proprietary solutions without any means for interoperability and data interchange. Each type of flight recorder required its own custom analysis platform. This lack of flexibility prevented users from taking complete advantage of advancements in technology and competition between vendors.

That is all changing with the adoption of IRIG 106 Chapter 10, the Digital On-Board Recorder Standard, the culmination of several years' cooperative effort by the Range Commanders Council, manufacturers and users. This new recording standard is leading to a revolution in the way airborne telemetry data is captured, recorded, analyzed and distributed by standardizing the digital data recording directory and data format for random access digital media. In addition to the


Figure 1

A "power user" of digital data recording, the Global Hawk UAV uses IRIG 106 Chapter 10 technology for mission imaging.

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standardized file structure and data format, IRIG 106 Chapter 10 provides well-defined control and download interfaces and secure erase procedures. Digital Data recording is used heavily in all manor of military system ranging from Apache helicopters to Aegis Missile Cruisers to UAVs like the Global Hawk (Figure 1).

## Broad Compatibility

The most obvious advantage of the new digital standard is the ability to take a recorded media cartridge from any vendor's flight recorder, download it via a standard interface to a PC, and analyze it with a compliant software package from any other vendor.

This compatibility greatly increases the return on investment in software packages, system integration and training. Previously, several staff years of effort were required to integrate a new vendor's recorder. Now, once an IRIG 106 Chapter 10-compliant recorder is integrated with an analysis system, only a minimal effort is required to integrate additional standard-compliant recorders.

Such inter-vendor compatibility increases reliability. Once tried and true analysis methods are established, they can be confidently reused with any standard-compliant recorder. There is no need to start again at the bottom of the learning curve with an entirely new proprietary system.

## Immediate Accessibility, Easy Distribution

Not only can a single software system analyze data from different recorders, but the converse is also true with the new standard: data from one recorder can be analyzed by many different software systems. This is especially important for airborne telemetry data, because many different parties typically require access to the data. For example, telemetry data from a test flight may be sent to several suppliers of the various components of the aircraft. Recipients can each employ their own standard-compliant decommutation and analysis systems.

A single user may also utilize multiple analysis systems for the same data. For instance, a laptop can be used to quickly verify data immediately after a flight, and then later a workstation can be employed to perform more extensive and detailed analysis. A principal advantage of digital technology is the ease of distribution. Captured as bits and bytes, data can be copied onto a wide variety of low cost media, including CDs and DVDs, and sent over data networks and the Internet. Data can also be posted on a secure server, allowing multiple users to easily access it.

IRIG 106 Chapter 10 requires the utilization of Telemetry Attributes Transfer Standard (TMATS), presented in Chapter 9, which provides meta-data tags to identify and describe all data. TMATS includes information on the signal sources, and the configuration of the recording equipment used to acquire the data. Because the TMATS tags are an integral part of the data, IRIG 106 Chapter 10 recordings cannot become unlabeled or mislabeled during copying, distribution and archiving. Figure 2 shows a functional overview of the IRIG 106 Chapter 10 standard.

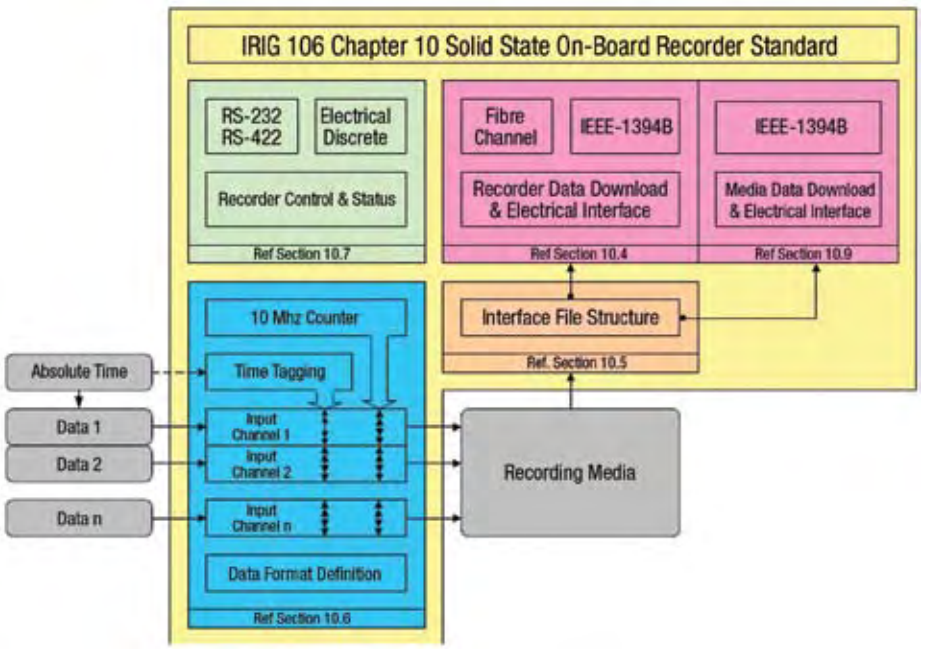


Figure 2

The IRIG 106 Chapter 10 standard supports acquisition of a wide range of signal types, including PCM, MIL-STD-1553, discrete data, video, computer generated and analog signals. The method of acquiring and multiplexing the digitized signals into the recorded data stream is fully defined for each signal type, ensuring compatibility with replay gear.

## Accurate Fusion of Many Signal Types

The standard supports acquisition of a wide range of signal types, including PCM, MIL-STD-1553, discrete data, video, computer generated and analog signals. The method of acquiring and multiplexing the digitized signals into the recorded data stream is fully defined for each signal type, thereby ensuring that compliant analysis and replay equipment will always recognize and correctly interpret the data. For users of analysis applications integrated with hardware-based data collection systems, the standard supports complete analog reconstruction of the original signal types while preserving accurate time coherency between channels.

IRIG 106 Chapter 10 also supports the trend toward simplification of airborne instrumentation. We increasingly see the combination of video, PCM and other signals, together with 1553 data, into the ultimate all-in-one recording system that conveniently offers fusion

Figure 3

Heim Data's D5000 system offers up to 256 Mbit/s total system data rate. These systems are compatible with both Heim Data format and the IRIG 106 Chapter 10 standard, including a compliant IEEE-1394b data download interface on the media cartridge.

and separation of all data types, with precise time-coherent analysis and playback easily achieved. Such single box solutions can replace two or more legacy recorders, with great savings in onboard resources and significantly improved performance.

## Time Coherency and Resolution

Time coherency is critically important for flight data recording, to ensure synchronization of data from multiple sources on the same aircraft, as well as to correlate with recorders located on the ground or in other aircraft. Digital technology has the advantage of recording timestamps based on an internal crystal controlled clock. IRIG 106 Chapter 10 defines the time source and a method of time tagging the data that allows high accuracy in both absolute time and in relative time between signal channels.

Companies like Heim Data have invested several years in developing hardware and firmware methods of providing accurate synchronization between data time tagging and the reference clock across multiple channel types. The time delay experienced by a signal between reception at the hardware input and actual time stamping is different for each type of signal channel. Therefore, careful attention must be given to accurate compensation of this time variance in order to maintain channel-to-channel coherency.

An example IRIG 106 Chapter 10 data recording system is Heim Data's D5000 system (Figure 3). With up to 256 Mbit/s total system data rate, this recording system employs media contained in interchangeable cartridges, allowing the user to quickly choose and load either rugged hard drive or solid state media at any time during the life of the equipment. These systems are compatible with both Heim Data format and the IRIG106 Chapter 10 standard, including a compliant IEEE-1394b data download interface on the media cartridge. The D5000 mainframe also has Gbit Ethernet data download capability and the media SCSI interface provides a high-speed output to other Heim Data download and signal reproduction systems that are fitted with media cartridge receivers.

The 10 MHz clock provides 100 ns time stamp resolution, significantly better than previous generation recorders. The absolute clock provides a supplemental timing method that is highly useful for correlating data captured on separate recorders, even at geographically separate locations. The accuracy of the absolute clock can be further enhanced by synchronizing the recorder's internal clock with time signals received from Global Positioning Satellites or other external reference clocks.

## Looking Forward

The new IRIG 106 Chapter 10 standard is accelerating the migration to digital recording, as users recognize the benefits of digital technology. However, universal adoption will not occur overnight, and vendors need to continue to support the recording and reconstruction of analog signals, video and audio. Many users have a large investment in analog technology and the benefit of digital technology does not always outweigh the cost of replacing legacy systems. This calculus is changing for some, as the availability of analog tapes decreases.

IRIG 106 Chapter 10 allows users to benefit from digital technology, without being dependent on a single vendor. By lowering the switching costs, users can augment their capabilities, or seek new solutions, as their needs and the available technology evolves, while still protecting their basic investment in software-based decommutation and analysis systems.

IRIG 106 Chapter 10 brings order to what has been a chaotic environment for users of first-generation digital recording systems. There is no longer the threat of expensive obsolescence or inferior performance through being tied to a single vendor's proprietary digital data format. The standard takes account of all steps in the acquisition process from signal source through to analysis software and provides an easily implemented means for interoperability and data interchange. This will bring comfort to the research, development and test community at large and encourage better products through healthy competition between vendors. ■

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# Onboard Network Improves Navy Ship Reliability

Reliability analysis is made easy by making effective use of a ship's high-speed, fiber optic LAN, coupled with powerful ability for real-time machinery performance data to be acquired, archived and analyzed by the diagnostic software agents.

Kevin Logan, President
MACSEA
Chuck Harrell, Marketing Manager
Advantech, eAutomation Group

Military Sealift Command (MSC), as part of the U.S. Navy, provides strategic sealift and ocean transportation for U.S. military forces. Its mission is to provide ocean transportation of equipment, fuel, supplies and ammunition to sustain U.S. forces worldwide during peacetime and in war. MSC operates more than 120 ships worldwide on a day-to-day basis, all crewed by civilian mariners.

As the United States continues to reduce the size of its military presence overseas, our military's readiness and rapid response capabilities depend increasingly on MSC. It is a matter of national priority that MSC ships be available at a moment's notice and perform reliably when called upon. MSC operates ships that provide combat logistics support to U.S. Navy ships at sea; special mission support to U.S. government agencies; pre-positioning of U.S. military supplies and equipment at sea; and ocean transportation of DoD cargo in both peacetime and war.



Recent crises have reinforced MSC's vital role as a major contributor in the execution of U.S. national strategy. Figure 1 shows an example MSC vessel, the USNS Patuxent, part of the Naval Fleet Auxiliary Force.

## Low Asset Costs and High Reliability

The Navy places strong emphasis on reducing the total ownership cost of its assets throughout their life cycle. Studies indicate that manning and maintenance


Figure 1

The USNS Patuxent is one of Military Sealift Command's fourteen Fleet Replenishment Oilers and is part of the 38 ships in the Naval Fleet Auxiliary Force.

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related costs consume the largest part of the operations and support budget and continue to grow most rapidly. Cost reduction efforts are therefore focused on reducing manning levels and implementing Condition-Based Maintenance (CBM) on future Navy ships.

The cost benefits of CBM strategies for machinery health monitoring have been clearly established in many industries, however, an effective CBM program can't be implemented without expense. Machinery condition must be measured via sensor instrumentation and assessed using special analytical methods, which often require special expertise. Specific CBM work tasks must be diligently performed and can generate significant crew workload requirements. With the trend toward reduced manning, there simply are not enough people to gather and analyze performance data on the multitude of machinery and equipment found aboard Navy ships. This situation has caused a needs gap within the Navy maintenance community.

## Automating Fleet-Wide CBM

Existing shipboard machinery automation systems are primarily designed for safety and protection. They also provide large amounts of data for equipment health monitoring; however, transforming massive amounts of data into actionable information for effective CBM remains an arduous task. The situation will be amplified on future all-electric Navy ships, as distributed, integrated power systems will include orders of magnitude more sensors than today's ships, creating increasingly complex maintenance requirements. Machinery performance monitoring and health assessment are areas where the exploitation of software agent technology will yield substantial near-term economic benefits to the Navy.

Software agents can be used to clone human intelligence, perform human-like reasoning, and interact with human clients. Agents can perform tedious, repetitive, time-consuming and analytically complex tasks more accurately and reliably than people. Software agents can serve as expert assistants in monitoring, troubleshooting and predicting failures in complex machinery processes in support of drastic manning reductions on future ships. Imparting intelligent processing functions into software agents will allow the Navy to leverage valuable knowledge across a geographically distributed ship fleet. Agents can be distributed when and where needed to enhance fleet operations, performance and readiness. Their intelligence can be upgraded remotely. The human-agent team can provide higher levels of platform readiness/reliability at far less cost than that of the equivalent human resource required to perform the same work.

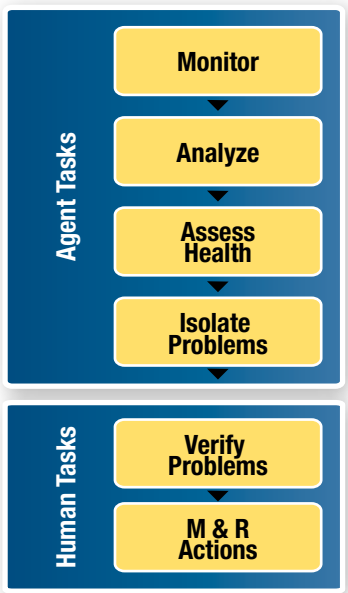


Figure 2

Illustrated here is the division of labor between software agents and humans for typical equipment health monitoring tasks. The agents automate the majority of these processes, reducing the human's role to fault verification and corrective action.

To facilitate such requirements, engineers at MACSEA have developed a software product called DEXTER that allows its customers to build and deploy machinery health monitoring software agents. The agents are designed to automate the majority of the data gathering and analytics associated with CBM. The software agents are deployed in machinery data networks and perform their work unobtrusively in the background, alerting maintenance and operations personnel when an equipment problem has been detected or predicted to occur in the near future. This allows expeditious isolation and repairing of existing problems and, through predictive analytics, the avoidance of future problems that could impact machinery reliability.

MSC has been one of the early adopters of MACSEA's intelligent software agent technology to support cost-effective CBM with minimally manned ships. DEXTER agents have been customized and deployed aboard MSC vessels for several years, primarily for diesel and gas turbine engine health monitoring.

## Intelligent Software Agents for CBM

Intelligent software agents automate the bulk of the work necessary to continuously monitor machinery health. They autonomously perform complex information processing tasks to identify impending failures and accurately predict remaining useful equipment life. Software agents can be deployed to automatically monitor and analyze hundreds of thousands of data points, while being integrated into existing automation system environments at relatively low cost.

Figure 2 illustrates the division of labor between software agents and humans for typical equipment health monitoring tasks. The six main CBM processes include data acquisition, equipment performance analysis, condition assessment, fault diagnosis and isolation, problem verification, and maintenance/repair action. As shown in Figure 2, the agents automate the majority of these processes, reducing the human's role to fault verification and corrective action.

Those human activities only become necessary after a problem has been identified by an agent, resulting in very significant savings in manpower required for CBM implementation. DEXTER agents can be created for any type of machinery systems for which sensor measurements are available. This technology allows

companies that have already invested in plant automation systems and process control software to further leverage these investments with advanced agent-based analytics. Figure 3 illustrates the distinction between Diagnostic Agents and Prognostic Agents.

***Diagnostic Agents:*** Diagnostic agents perform real-time assessment of existing alarm conditions. Their automatic fault diagnostics provide troubleshooting assistance to maintenance personnel, directing them to the most likely problems causing the alarms. The agents will reduce troubleshooting time and help restore normal operations as quickly as possible, minimizing the cost of any process disruption. All diagnostic events are logged, allowing a management review of equipment reliability over any operating time interval. A distinguishing feature of diagnostic agents is their real-time assessment of behavioral anomalies of plant machinery. The probabilistic assessment of equipment faults can be particularly useful to new maintenance personnel that may be unfamiliar with plant operations. Their job performance and, in turn, plant reliability, stands to benefit from the knowledge and experience of the team of experts used to develop the diagnostic knowledge base.

***Prognostic Agents:*** Prognostic agents predict machinery problems at their earliest stage of development. Developing equipment problems can often be discovered by degrading performance trends in historical data. Prognostic agents automatically perform statistical trending analysis to detect abnormal machinery performance trends. These agents are important tools for maintenance personnel to implement effective Condition-Based Maintenance (CBM). The predictions of future machinery faults include estimated time to failure, and as such, can help determine when maintenance should be carried out. By predicting machinery problems before they occur, unexpected breakdowns can be avoided. In the absence of significant trends, equipment overhaul periods may be rationally extended, thereby eliminating unnecessary maintenance work. The ability to predict future maintenance requirements improves maintenance planning, cost management and plant reliability. Maintenance and repair decisions can be tied to actual plant operating conditions based on the severity of degrading trends and predicted plant problems.

## Neural Network-Based Diagnostic Reasoning

During the past several decades, scientists developed computer models of biological neural networks that can learn and perform brain-like functions. These models, referred to as artificial neural networks, are able to learn from examples and are particularly useful for certain tasks, such as pattern recognition. DEXTER agents use neural networks for their diagnostic and prognostic reasoning about machinery faults. The software agent's neural network automatically learns to associate patterns of alarm conditions with the machinery faults.

Missed diagnostic calls and false calls translate directly into added maintenance costs, either from unexpected machinery failures or unnecessary maintenance activities. The robustness of a diagnostic system therefore directly impacts maintenance expenditures, as well as equipment reliability. DEXTER's neural networks are tolerant of noisy or incomplete input patterns, making their diagnostics more robust than those developed from logic or rule-based approaches. Even if one or more symptoms are missing, DEXTER still identifies the most probable faults based on all available evidence.

## Reliable Hardware for Harsh Environments

The diagnostic system that monitors the reliability of the machinery has to be extremely reliable itself. A typical shipboard environment is about as harsh as it gets on a computer system that needs to run continuously for extended periods of time. Corrosion, high vibration, low quality power, frequent power interruptions, high temperature, dust and dirt are some of the factors that can destroy most electronic equipment. While the DEXTER agent server computer isn't subject to crashing ocean waves, it is subject to all of the other aforementioned factors. MACSEA thoroughly investigated commercial industrial grade computing platforms over ten years ago and selected the Advantech IPC 6806 series computer to host its shipboard diagnostic software.

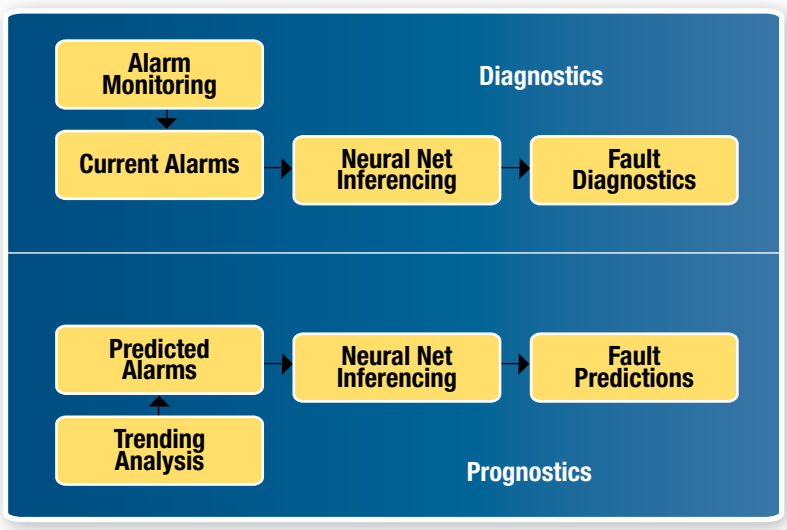


Figure 3

Diagnostic agents perform real-time assessment of existing alarm conditions. Their automatic fault diagnostics provide troubleshooting assistance to maintenance personnel, directing them to the most likely problems causing the alarms. Meanwhile, prognostic agents predict machinery problems at their earliest stage of development.

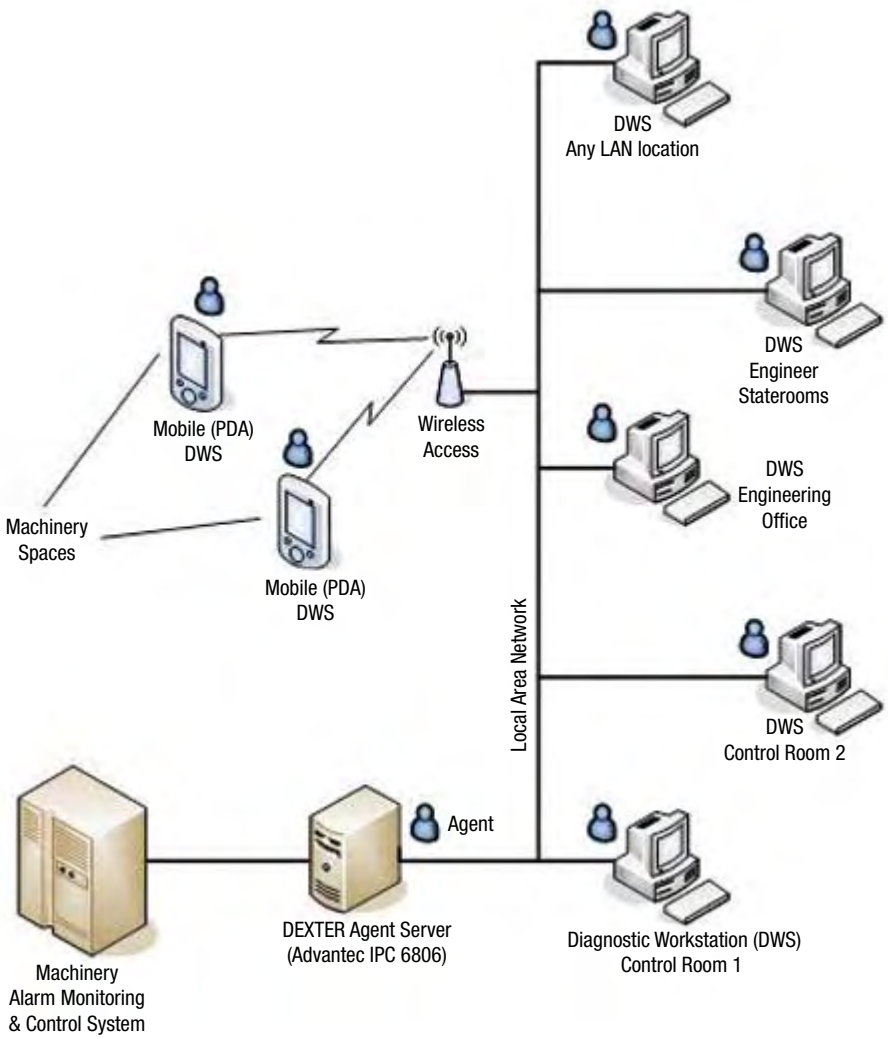


Figure 4

This is a typical shipboard configuration for deploying DEXTER machinery diagnostics. The DEXTER Server (IPC 6806) interfaces directly with existing machinery alarm monitoring and control systems through a serial or Ethernet connection. That enables real-time machinery performance data to be acquired, archived and analyzed by the diagnostic software agents.

As it turned out, it was the right choice, as this workhorse has performed extremely reliably on over 40 ship installations made over a ten year period. "The Advantech IPC computers have worked reliably on some ships for over ten years without a problem," reports Robin Osmer, MACSEA field service technical manager. "The locations where we install them aren't the best for computer equipment, which is, in most cases, a small enclosed area inside a control console. Even with poor air flow and high temperatures, these computers just keep on working."

Figure 4 illustrates a typical shipboard configuration for deploying DEXTER machinery diagnostics. The DEXTER Server (IPC 6806) interfaces directly with existing machinery alarm monitoring and control systems through a serial or Ethernet connection. This allows real-time machinery performance data to be acquired, archived and analyzed by the diagnostic software agents. The DEXTER Server is also connected to the ship's high-speed, fiber optic LAN, which serves as the ship's data highway.

Diagnostic workstations running DEXTER client software are distributed throughout the ship and allow engineers real-time access to plant data and diagnostic agent results. By transmitting real-time machinery performance data across the LAN, DEXTER provides a very convenient and inexpensive means for the engineers to keep a close watch on the machinery plant from the comfort of their staterooms, which are typically several decks away from the control room. When an abnormal event occurs in the middle of the night, they can check it out a few steps away on their workstation, instead of having to walk down several flights of stairs to the control room.

## Low-Cost Solution for Enhanced Gas Turbine Monitoring

On one particular class of DEXTER-installed ships, the MSC engineers wanted to enhance their monitoring of the main gas turbine engines by measuring the inlet air filter differential pressure. Inlet air has a large impact on gas turbine performance, but for some reason, this particular parameter was not instrumented during ship construction as part of the normal automation system. After receiving a high cost estimate from the control system vendor, MACSEA was approached to suggest a solution. A simple design comprised of an ADAM 4017 8-channel analog input module, small power supply and enclosure box was subsequently installed and tested aboard the USNS Supply. The ADAM 4017 signals were fed directly into the DEXTER Server for display and analysis. This simple, low-cost solution using the ADAM modules is currently being installed on three additional MSC gas turbine ships. ■■

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# Processor PMCs Get Faster, More Flexible for Mil Apps

As increasingly sophisticated military systems are built in the processor PMC form-factor, these modules are getting faster and more flexible with lots of specialized I/O and lower power consumption.

Ann R. Thryft,
Senior Editor

Military engineers are incorporating processor PMC technology in a growing number of integrated applications that require high performance, lots of I/O throughput and low power consumption. This compact, industry standard form-factor packs a lot of performance and functionality into a very small space. By taking out the computing core of an SBC—the processor and memory that need upgrading more frequently—and putting it on an easily swapped out module, the SBC's life can be extended and much of the technology investment can be preserved.

Meanwhile, the base board becomes a platform for slower-changing I/O or I/O created with custom designs. That's how processor PMCs (PrPMCs) accommodate the long design cycles of many military systems while still allowing new technology insertions to deliver flexibility, performance and cost control.

Processor PMCs have come a long way from their origins as a card with just a processor, main memory and a PCI interface. Today, they integrate some of the fastest CPUs available and can be used for highly specialized processing functions. Dual-core high-speed CPUs, PCI-X bus interfaces, graphics interfaces for the increasing amount of visual data in military systems and high-speed system, memory and I/O interfaces are some of the possibilities with current PrPMCs.

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courtesy of: U.S. Airforce

Figure 1

A wide range of military systems, such as signal processing, software defined radio, flight computers and command/control/communications, depend on high-performance PrPMC cards as their computing cores. The MQ-1 Predator unmanned aerial vehicle provides real-time "eyes in the skies" to ground commanders for identifying enemy activities.

Each year more of them come with multiple Fast Ethernet and Gigabit Ethernet ports. Many even offer specialized communications protocol and packet processing as military networking and communications functions become more pervasive and important in defense system design.

Processor PMCs are flexible in other ways, too. They are often mounted on non-standard base boards of many different sizes and shapes and are not limited to standard 6U VME and 6U CompactPCI applications. On the local PCI bus they can act as either its host, in "monarch" mode, or as a peripheral, in "non-monarch" mode.

In many highly integrated defense applications such as flight computers, software defined radio and command/control/communications systems, signal processing and control subsystems must deliver both low power and high I/O throughput (Figure 1). Today's PrPMCs meet both of these conflicting requirements with low-voltage processor options, sophisticated power management schemes and the use of lower-power, high-performance microcontrollers with a rich mix of peripherals. Others let designers program and reprogram a processor's speed to fine-tune the board's power consumption so it only uses the very minimum needed for a particular application.

As military systems get more connected and networked, PrPMCs will continue to deliver the computing power, modularity, connectivity and scalability that defense engineers have come to expect from this mezzanine form-factor.

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# Technology Focus:

# Processor PMC Boards Roundup

## Dual PowerPC Card Features Programmable Processor Speed

Each defense application has its own unique requirements for power consumption and operating speed. What if military engineers could change the processor's speed to lower power consumption, and then reprogram it when requirements change? They can do exactly that with the PMC-106 single/dual MPC7447/A PowerPC Processor PCI mezzanine

card (PrPMC) from Curtiss-Wright Controls Embedded Computing. The processor's core frequency is software-programmable to operate between 500 MHz and 1 GHz. By reducing operating frequency, the PMC-106's power consumption can be reduced to the minimum possible for a given application.

The VITA 32-compliant PMC-106 PrPMC provides up to 256 Mbytes of ECC-protected DDR-250 SDRAM and 64 Mbytes of flash. The card's PCI-X interface supports 64-bit/133 MHz transfers. It is backward compatible with 32-bit or 64-bit host carrier cards from 33 to 133 MHz. The module can act as the host (monarch) of the local PCI bus or as a peripheral (non-monarch) on the local PCI bus.

A single 10/100/1000Base-T Ethernet port as well as two EIA-232/422 asynchronous serial ports are available through the Pn4 connector to the rear panel. Two thermal sensors, 8 Kbytes of FeRAM, JTAG emulation ports and six discrete LVTTL signals round out the peripherals. The PMC-106 does not support front-panel I/O, but uses the Pn4 connector to route out all rear panel I/O. The card's Discovery II bridge chip provides a four-channel DMA controller, typically used for managing transfers between processor node memory banks and transfers to and from PCI devices. The board supports VxWorks 5.5, Tornado 2.2 and Linux kernel 2.4. Price starts at $4,000.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

## PowerQUICC III Card Provides Protocol and Packet Processing

The protocol and packet processing needed in applications such as radio network controllers and base transceiver stations used to be delivered strictly at the system box level, but PrPMCs enable developers to pack a lot more specialized processing into a smaller space. Now some PrPMCs bring dedicated protocol and packet processing onto the PrPMC itself. An example is Emerson Network Power Embedded Computing's Pm8560, an octal E1/T1 PrPMC protocol engine based on the MPC8560 PowerQUICC III communications controller. The card provides a simple way to add protocol processing and signaling capability to communications systems equipped with PMC or PTMC expansion slots.

The Pm8560 features 512 Mbytes of SDRAM, 32 Mbytes of flash and a multichannel T1/E1 interface. The MPC8560 operates at 800 MHz and combines a PowerPC Book E e500 core with a multichannel Communications Processor Module (CPM). It features a single precision floating-point unit and delivers peak performance of 1850 Mips. The RISC-based CPM features

three fast serial communications controllers, two multichannel controllers, four serial communication controllers, a serial peripheral interface and an $I^2C$ interface. The MPC8560 also includes a 64-bit PCI/X/PCI controller, a RapidIO port and a pair of 10/100/1000 Ethernet controllers.

The Pm8560's mezzanine interface complies with IEEE 1386.1 (PMC) and provides a subset of the PICMG 2.15 PTMC Configuration 2 features. The Pm8560's E1/T1 interfaces reside on a rear transition module installed on the baseboard. After processing the data and converting it to a packet format, the Pm8560 can send it back to the baseboard for additional processing or transmission over the backplane, or transmit the data directly to a packet network via its 10/100/1000 Gigabit Ethernet port. Software support includes MontaVista Carrier Grade Linux CGE3.1.

Emerson Network Power
Embedded Computing
Madison, WI.
(608) 831-5500.
[www.artesyncp.com].

## PMC/XMC Comms Controller Features 1.5 GHz MPC8548E

When PrPMCs first emerged several years ago most were pretty simple, containing only a processor, main memory and a PCI interface. Back then, no one expected them to offer the same leading-edge computing performance as their larger 6U cousins. But today's crop of PrPMCs integrate some of the fastest CPUs

available, and a whole lot more. An example is Extreme Engineering Solutions' XPedite5200, a high-performance PMC/XMC communications controller and the first PrPMC to use the 1.5 GHz MPC8548E PowerQUICC III. The processor's integrated 64-bit 133 MHz PCI-X, DDR-2-533 SDRAM, PCI Express/Serial RapidIO and four Gigabit Ethernet interfaces make the XPedite5200 an optimal solution for communications processing.

The processor also includes a 512 Mbyte L2 cache and double precision floating point unit as well as two serial controllers and two $I^2C$ controllers. Memory provided on the board is up to 2 Gbytes of DDR-2-533 SDRAM and up to 256 Mbytes of NOR flash, up to 2 Gbytes of NAND flash and up to 2 Kbytes of serial EEPROM. The XPedite5200 has two front-panel Gigabit Ethernet interfaces and supports two more via the P14 backplane connector.

When used as a VITA 42 XMC module, either the x8 PCI Express or x4 Serial RapidIO interfaces can be used, in parallel to or in substitution for the PCI-X interface. With software supplied by Extreme, the XPedite5200 can be installed on standard VME and cPCI platforms as well as custom motherboards that support PMC sites. Operating temperature is 0 to 55°C from a 3.3, 5 or 12V power supply. Linux, VxWorks, Integrity and QNX support packages are available. Pricing starts at $4,100 in low quantities for a module with 1 Gbyte of DDR-2 SDRAM and 128 Mbytes of NOR flash.

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## PrPMC Card Features 1.4 GHz Pentium M LV

Demanding applications such as flight computers, software defined radio and command, control and communications systems have several needs in common including high performance, low power and a Windows XP graphical user interface. Where those are equally top priorities, it's hard to beat a PrPMC architecture that can accommodate all three. One example is GE Fanuc Embedded Systems' PSL09 PrPMC, which brings the high performance of Intel's 1.4 GHz Pentium M LV to PCI-based military applications. For extremely low power requirements, the PSL09 is

also available with a Celeron M ULV processor running at 600 MHz or 1 GHz.

The PSL09 supports a 33/66 MHz PCI bus and incorporates sophisticated power management technology, a VGA interface, up to 2 Mbytes of L2 cache and up to 256 Mbytes of 333 MHz DDR SDRAM with optional ECC. Both monarch and non-monarch modes are supported. The board provides extensive connectivity with four USB 2.0 ports, two serial ATA channels and two Fast Ethernet ports. Upon request, the PSL09 features PICMG 2.15 compatibility with the added option of one or two Fast Ethernet links through the Pn4/Jn4 connector. The PICMG 2.15 option enables the PSL09 to operate with CompactPCI 2.16 and ATCA carrier boards.

Other options include 256 Mbytes of flash with EIDE interface. Operating temperature range is 0 to +50°C. An extended temperature version is available, operating at -40° to +55°C. The PSL09 supports Linux, VxWorks and Windows XP. Pricing starts at $2,140 in single quantities.

GE Fanuc Embedded Systems
Albuquerque, NM.
(505) 875-0600.
[www.gefanucembedded.com].

## PrPMC is Conduction-Cooled, Consumes 3 Watts

For small, ultra-low-power applications, shaving down the amount of power consumption in a subsystem can be tough. That's why Interface Concept designed its IC-PQ2-PMCb PrPMC module to consume only 3 watts, by taking advantage of Freescale's PowerQUICC II controllers, known for both low power consumption and high levels of integration. The module contains the MPC8270 PowerQUICC II processor running at up to 266 MHz. The MPC8270 couples a 603e core with a RISC communication processor and three Fast Ethernet controllers, as well as a 16 Kbyte instruction cache and 16 Kbyte data cache, 64 Kbytes of onboard fast dual-port SRAM, MMU and FPU capabilities and DMA channel controllers.

The rugged PrPMC offers 64 or 128 Mbytes of shared ECC SDRAM, 128 Kbytes of SRAM, 8 or 32 Mbytes of NOR flash and 32 Kbytes of SPI EEPROM. I/O includes up to three 10/100 TX auto-sensing Fast Ethernet ports that are routed to the rear connector, as well as four high-performance serial controllers. A 64-bit PowerPC local bus is usable by the host via the 32-bit PCI bus through a PowerPC-to- PCI bridge. The board can be used in monarch, non-monarch or stand-alone modes.

Options include a 128 or 256 Mbyte soldered flash disk, and a reverse Pn3 to mezzanine

board connector. Software support includes firmware with BIT, as well as board support packages (BSPs) for VxWorks and Linux environments. Supported communications protocols include Ethernet-TCP/IP, PPP, BOOTP, TELNET, TFTP, HDLC and HTTP server. Pricing starts at $2,995.

Interface Concept
Briec de l'Odet, France.
+33 (0)2 98 57 30 30.
[www.interfaceconcept.com].

## Pentium M Card Sports 400 MHz System Bus

Processor PMCs have spurred on an interesting design phenomenon among vendors that make both PrPMCs and larger SBCs. Because PrPMCs by definition comprise the central computing elements of an SBC, board designers can easily recast that design into other form-factors such as CompactPCI.

Exemplifying that trend is a PrPMC board from Mercury Computer Systems that is also available in a 6U CompactPCI form-factor.

Based on the Pentium M 1.4 GHz Pentium M processor with 1 Mbyte on-die L2 cache, the PrPMC Cheetah PCR-150 incorporates up to 1 Gbyte of single-channel 64-bit DDR 333 SDRAM with ECC and the Intel 855GME memory controller, which supports a 400 MHz system processor bus. A 1 Mbyte firmware hub and a side accessible Type I or II CompactFlash socket are provided. Monarch and non-monarch modes are supported.

An Intel 82546EB provides PICMG 2.15 PTMC-compliant dual Gigabit Ethernet links on the PMC Pn4 connector through a 64-bit, 66 MHz PCI-X bus on the Intel 6300ESB I/O controller hub. A PLX PCI6540 PCI-X-to-PCI-X bridge provides 64-bit 133/100/66 MHz PCI-X or 66/33 MHz PCI bus operation on the PMC interface. Other interfaces include a front panel VGA HD15 interface, a 1 Mbyte firmware hub and two USB 2.0 ports. On the PMC Pn4 connector are a SATA 150 interface, two more USB 2.0 ports and two serial ports. The board supports operating temperatures of 0 to 55°C. An optional PMC arbiter on Pn4 supports four external PCI master devices. Operating system support includes Windows 2000/XP, FreeBSD, Linux, Solaris and VxWorks. Price is $1,995 in OEM quantities.

Mercury Computer Systems
Chelmsford, MA.
(978) 256-0052.
[www.mc.com].

## PrPMC Weds 1.4 GHz PowerPC with 1 Gbyte SDRAM

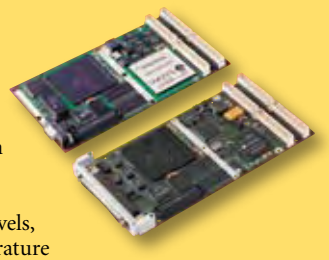
As the originator of the Processor PMC standard, Motorola Computer Group has maintained a steady stream of PrPMC products over the years. Instead of treating PrPMC as a trailing-edge standard, its strategy has been to share the basic core computing design between corresponding PrPMC and VME SBCs. Motorola's latest, and fastest, PrPMC offering is the PrPMC6001, a single-width PCM featuring an MPC7448 PowerPC G4 processor built with AltiVec technology that enables speeds of up to 1.4 GHz, along with up to 1 Mbyte of L2 cache.

A highly integrated Marvell Discovery III system controller gives the processor high-speed access to up to 1 Gbyte of external ECC DDR SDRAM with Motorola support and up to 256 Mbytes of flash. Dual independent Gigabit Ethernet interfaces, one of which has optional SerDes support, are routed to the PMC connector. The card provides a 64-bit/66-133 MHz PCI-X interface, a PTMC-compliant P4 connector and dual serial interfaces. It can run in monarch or non-monarch mode.

The PrPMC6001 is VITA 32 and VITA 39 (PCI-X Auxiliary) compatible. It supports VxWorks 5.5 and 5.5.1, certain carrier grade Linux distributions and kernel.org 2.6.10. List price is $1,695 for the PrPMC6001M-001 with 512 Mbytes of DDR SDRAM and $1,955 for the PrPMC6001S-001 with 1 Gbyte of DDR SDRAM.

Motorola Embedded Communications Computer Group
Tempe, AZ. (602) 438-3000. [www.motorola.com].

## 450 MHz PowerQUICC II Card Offers Five Ruggedization Levels



When developing defense applications, it can be really handy to the military system designer to have a choice of ruggedization options. With that need in mind, Radstone offers its PrPMCQ2 in five ruggedization levels, from a convection-cooled operating temperature range of 0 to 55°C at one end of the spectrum to a conduction-cooled range of -40° to +85°C at the other end.

Built around the 450 MHz Freescale MPC8280 PowerQUICC II processor, the PrPMCQ2 features a communications processor at up to 300 MHz and memory interfaces at 100 MHz. It provides 32 Mbytes of SDRAM and 16 Mbytes of flash, is 64-bit/66 MHz PCI 2.1-compatible and provides four general-purpose I/O lines. The PrPMCQ2 also offers four high-speed serial channels, capable of RS-232/422/485 operation (software selectable), and configurable for synchronous or asynchronous operation. Two additional channels provide asynchronous capability useful for development debug and deployed operation on lower-speed traffic lines. A single 10/100BaseT Ethernet port completes the array of communications options.

The PrPMCQ2 can function in either monarch or non-monarch modes. Its power consumption is extremely low, only 5W typical. BSPs and Enhanced Support Packages (ESPs) are available for VxWorks and Integrity. Pricing starts at $2,160.

Radstone Embedded Computing, part of GE Fanuc Embedded Systems, Billerica, MA. (800) 368-2738. [www.radstone.com].

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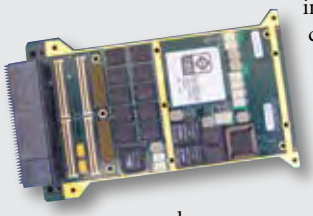
## VPX Board Serves Up Dual 2 GHz PA Semi CPUs

High compute density is top priority for a variety of today's advanced military programs. This year will probably see many compute-intensive offerings in the VPX-REDI form-factor. An early offering along such lines is Extreme Engineering's XPedite8070, a high-performance 3U VPX-REDI single board computer that is ideal for ruggedized systems requiring high-bandwidth processing and low power consumption. With two PA Semi PA6T cores running at up to 2.0 GHz while dissipating less than 17W, the PA6T-1682 delivers optimum performance per watt. The PA Semi PA6T-1682 PWRficient integrated platform processor combines dual PA6T cores and high-performance communication to two DDR2 SDRAM channels and a plethora of network interfaces.



XPedite8070 supports two separate channels of up to 1 Gbyte each of 400 MHz DDR2 ECC SDRAM, as well as up to 1 Gbyte of NAND Flash. XPedite8070 provides the option of utilizing PCI Express, 10 Gigabit Ethernet XAUI and Gigabit Ethernet P1 interconnects. XPedite8070 also supports dual Gigabit Ethernet, GPIO, I2C, PMC I/O, XMC I/O, and dual RS-232/RS-422 ports out the P2 connector. To the system designer, XPedite8070 provides a feature-rich solution to support the next generation of rugged embedded applications. Both a VxWorks Board Support Package (BSP) and a Linux 2.6 LSP are available. Single quantity pricing for XPedite8070 starts at $7,800 with large program/OEM pricing closer to $5,000, depending on volume, memory and processor configurations. The XPand1000 development chassis is available for $2,000.

Extreme Engineering Solutions, Middleton, WI. (608) 833-1155. [www.xes-inc.com].

## Motion Control IC Does Advanced Stall Detection


The new paradigm for military motor control systems is smaller, high-precision motors and more of them. Feeding that trend, Performance Motion Devices, Inc. announces the Magellan MC55110 single-axis, single-IC Motion Processor with automatic stall detection. This flexible device, designed specifically for step motor control, alerts the user when the motor has lost steps during motion. Losing steps (stall) typically occurs when the motor's motion has been obstructed, or a system failure has occurred.

The advanced functionality of the Magellan MC55110 allows the chip to actively monitor the targeted and actual position, and detect any number of motion errors that can result in a stall condition. Automatic stall detection operates continuously once it has been initialized by the user. To initiate stall detection, the host simply specifies the number of encoder counts per step The Magellan MC55110 Motion Processor is driven by a host microprocessor using an 8 or 16-bit parallel bus, CANbus 2.0B, or an asynchronous serial port. In addition to automatic stall detection, it provides advanced motion features such as programmable PID filter with velocity and acceleration feed forward, 32-bit position error and 50-µsec loop time. The MC55110 is available now. Prices start at $24 in OEM quantities.

Performance Motion Devices, Lincoln, MA. (781) 674-9860. [www.pmdcorp.com].

## CompactPCI Express CPU Board Dresses for 3U

Marrying the strengths of CompactPCI and PCI Express, the emerging CompactPCI Express architecture is winning mindshare in military, avionics and homeland security applications. Claiming to be the first such board in a 3U flavor, One Stop Systems has introduced its CompactPCI Express Pentium M CPU Board. Designed for a CompactPCI Express Type 1 system slot, it features a Pentium M processor with Intel 915 chipset. Passive and active cooling options are available, as is the choice to install a standard 1.8-inch parallel ATA HD or conventional CompactFlash. Regardless of mass storage choice, the CPU remains just 4HP wide. The board provides a full I/O, including Gigabit Ethernet, integrated COM port, triple USB 2.0 and PS-2 mouse/keyboard interfaces, which connect directly to the board. Additional features include LVDS, USB, Serial ATA, and 4x 1PCIe lanes. A 2 Mbyte L2 cache and 2 Gbytes of DRAM complement the board's capabilities.

An optional rear I/O module gives users a single rear access to all external cables. Fully compatible with existing operating systems and application software, the CPU is also fully I/O compatible with existing solutions based on the CompactPCI standard. Available now, the OSS CompactPCI Express Pentium M CPU Board lists at $3,995 in OEM quantities.

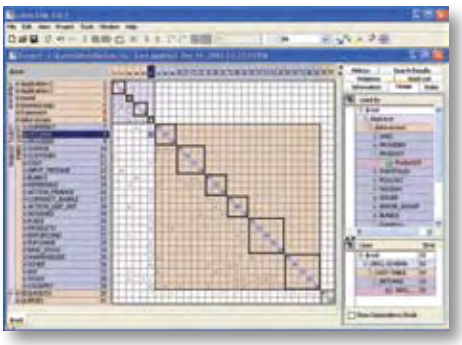
One Stop Systems, Escondido, CA. (760) 745-9883. [www.onestopsystems.com].

## Remote Video System Aids Net-Centric Ops

Gone are the days when remote video intelligence of UAV and similar assets required a fixed terminal. Now all the electronics and computing for such tasks can be integrated into a portable compute platform. Along just such lines, L-3 Communications announced its VideoScout-MC, a highly portable video exploitation and management system with an integrated L/C- or L/S-band receiver to directly receive video and telemetry data from manned or UAV systems.

Developed for special operations and warfighters on the front line, VideoScout-MC provides mobile and INTEL dismounted personnel with an "all-in-one" system to receive, exploit, archive, search, retrieve and disseminate critical video data across the battle space. The system includes an integrated L/S- or L/C-band receiver and antennas in a ruggedized, portable laptop running the Windows operating system. VideoScout-MC can receive data from L-band systems, such as the Dragon Eye, Raven and Pointer; S-band systems, including the Scan Eagle and Silver Fox; and C-band systems, including the Predator, Shadow, Hunter and LITENING Pod. Once the video has been received, warfighters can add "knowledge" to the captured video by annotating, extracting images, creating short clips and disseminating video anywhere across the battle space. VideoScout-MC deliveries will begin the first quarter of 2007.

L-3 Communications, Reston, VA. (703) 434-4000. [www.l-3com.com/apd].

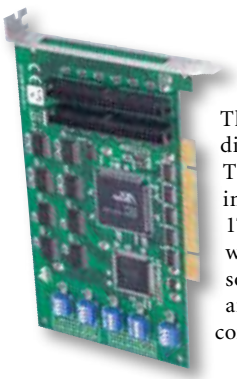


## Tool Prevents Software Architecture Erosion

Military embedded architectures are power users when it comes to code size and complexity. To help tame the beast, Lattix has announced the release of its newest solution, Lattix LDM 3.0. With this major release, Lattix enables managers, architects and developers to visualize, specify and maintain the architecture of a complex enterprise software system.

Lattix pioneered the Dependency Structure Matrix (DSM) approach, which uses dependencies to create an accurate and scalable blueprint of complex, mission-critical software applications. With Lattix LDM 3.0, it is now possible to apply this approach for systems that span different domains, from the database to services and applications. Lattix LDM 3.0 delivers effective architecture governance by providing the means to specify and test the architecture, detect violations during development and prevent further architectural erosion. Lattix LDM 3.0 is the most comprehensive architecture management solution, offering Java, C/C++, .NET, Oracle, Hibernate and LDI modules. Lattix LDM 3.0 also provides support for full Web-based reporting of architectural metrics, violations and incremental changes. Shipping now, Lattix LDM 3.0 is available in three editions, starting at $495 for the Professional Edition. A free evaluation license is also available for download.

Lattix, Andover, MA. (978) 474-5022. [www.lattix.com].



## Digital I/O PCI Card Has 48 Channels

As military applications pack in more and more types and amounts of sensor interfaces, the demand for digital I/O density is rising sharply. The eAutomation Group of Advantech introduces the PCI-1739U 48-channel digital I/O universal PCI card for both 3.3 V and 5 V PCI bus signaling. The PCI-1739U uses popular Opto-22-compatible 50-pin connectors for interfacing to many signal conditioning and termination options. The PCI-1739U has an interrupt function that can output a digital signal synchronized with an internal PC interrupt generated by the card. Other features include software configurable digital I/O channels, 0 to 65°C operating temperature and digital output status read-back. The power-on state of the outputs can be configured via dipswitches.

The PCI-1739U is a 48-bit DI/O card with PCI bus, and provides 48 bits of parallel digital input/output. It also emulates mode 0 of the 8255 PPI chip, but the buffered circuits offer a higher driving capability than the 8255. The I/O bits are divided into six 8-bit I/O ports: A0, A1, B0, B1, C0 and C1. Ports can each be configured as either input or output via software. The PCI-1739U starts at $195 and is available for purchase directly from Advantech.

Advantech, eAutomation Group, Cincinnati, OH. (800) 205-7940. [www.eAutomationPro.com].

## Fanless Micro PC Boasts Dual LANs

Fans are a no-no in most military applications. They can't tolerate the "single point of failure" that a fan represents. With that in mind, WIN Enterprises has announced the PL-01030, a compact, low-power, high-performance device that can be used as an entry-level micro PC embedded computer. Fanless operation also makes it attractive for harsh environment applications.

The PL-01030 features an AMD Geode LX800 500 MHz low-power processor, as well as two 10/100 Ethernet LANs, four USB 2.0 ports, four COM ports, CompactFlash and LPT I/O. The lightweight chassis is dust-proof, in compact size of just 8 and 1/8 inches (218 mm) in height. The unit draws only 12W, 5V @ 2.4A power consumption. Also featured are a VGA connector, mic input and one speaker output. The PL-01030 is available with a choice of Intel and Realtek LANs. Single unit prices range from $385 to $392, depending on LAN configuration.

WIN Enterprises,
North Andover, MA.
(978) 688-2000.
[www.win-ent.com].

## Thermal Gap Filler Cools Hot PCB Components

Military applications are in a pickle when it comes to thermal design challenges. On the one hand they're screaming for faster computer muscle—which means more power to dissipate. On the other hand, the strict thermal requirements and an aversion to cooling with fans make for some tricky cooling problems. Serving such needs, MH&W International has introduced Softtherm 86/200 material for providing an ultra-soft, thermally conductive gap filling interface between hot PCB components and their heat spreaders. Softtherm 86/200 has a very low 10 Shore 00 hardness.

The material can blanket over multiple components of differing height, contours and planarity. It is especially useful on fragile components sensitive to high pressure, or when only very low mounting pressure is available for attaching a heat-spreading device. Softtherm 86/200 material features a highly elastic, structurally secure silicone filled with ceramic particles. 86/200 is UL rated 94V-0 and has a TML (total mass loss) under 0.40%. It can be used in application temperatures from -60° to 200°C and with heat pipes, spreader bars, heat sinks and other cooling hardware. Pricing for the material starts at $0.10 for 1-in2 parts, 0.5 mm thick, in high volume orders.

MH&W International, Mahwah, NJ. (201) 891-8800. [www.mhw-thermal.com].

## Serial I/O Module Is Optically Isolated

USB ranks among the serial bus technologies approved for use by the DoD for defense applications. Marrying USB to legacy serial coms is ACCES I/O Products' Model USB-IIRO4-2SM. This dense multifunction device incorporates four optically isolated digital inputs, four Form C (SPDT) electromechanical relay outputs, and two RS-232/422/485 serial communication ports—all packaged in a small, rugged, industrial enclosure. This USB device is an ideal solution for adding portable, easy-to-install, digital and serial capabilities to any PC or embedded system with a USB port. It is fully compatible with both USB 1.1 and USB 2.0 ports. Hot-plug functionality allows for quick connect/disconnect whenever you need additional I/O on your USB port.

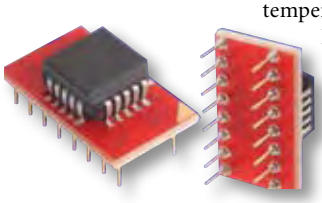
The board measures just 3.550 by 3.775 inches and ships inside a steel powder-coated enclosure with an anti-skid bottom. A DIN rail mounting provision is available for installation in industrial environments. What makes the OEM option unique is that its PCB size and pre-drilled mounting holes match the PC/104 form-factor—without the bus connections. The USB-IIRO4-2SM is priced at $249 OEM and volume pricing is available.

ACCES I/O Products, San Diego, CA. (858) 550-9559. [www.accesio.com].

## Adapter Weds 20-pin PLCC ICs to 16-pin DIP Footprints

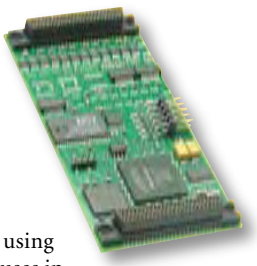
Obsolescence remains a critical problem in military system designs. One of the challenges is populating legacy board designs with the latest and greatest IC packages. That gets tricky when you're trying to fit modern PLCC-packaged devices into DIP board slots. Addressing that need, Aries Electronics has introduced a RoHS-compliant version of its 20-pin PLCC IC to 16-pin DIP Correct-A-Chip adapter. The new adapter is a cost-effective way of converting a PLCC-packaged type clock chip to a DIP footprint without changing the PCB layout.

The adapter features a PLCC clock chip on top with pin counts from 1 through 20 pins, and has a 1- through 16-pin DIP clock chip on the bottom. The design is unique in that it is slightly offset to avoid typical bypass capacity placement. The body of the adapter is constructed of a 1.56 mm (.062 inch) thick, glass-filled IS-410 material with one ounce of copper traces on both sides. The male pins are brass alloy 360 with 10 µ-inch minimum gold plating per MIL-G-45204 over 100 µ-inch minimum nickel plating per SAE-AMS-QQ-N-290. The maximum operating temperature is 221°F (105°C). Pricing for a new RoHS-compliant PLCC to DIP adapter is $6.17 each in quantities of 500.



Aries Electronics, Frenchtown, NJ. (908) 996-6841. [www.arieselec.com].

## Digital I/O Module Boasts Cyclone II FPGA



In adaptive computing applications, which are slowly increasing in the military, developers can develop and store their own instruction sets in an FPGA. Typical applications include specialized communication systems over RS-422/485 networks and analysis of acquired data using specialized mathematical formulas. With these uses in mind, Acromag has introduced the IP-EP200 series of Industry Pack digital I/O modules that implement the user-configurable Altera Cyclone II FPGA, as well as digital I/O for a variety of signal types.

Different models in the series provide 24 differential RS-485, 48 bi-directional TTL or 24 LVDS digital I/O signals. All models feature the Cyclone II EP2C20 FPGA with 20 K logic elements, 240 Kbytes of RAM and 26 (18 x 18) embedded multipliers. An Engineering Design Kit and a DLL driver software package for compatibility with Microsoft, Visual C++ and Visual Basic are available, as are C libraries for VxWorks and QNX. Prices start at $1,000. A combination model that pairs 24 TTL with 12 RS-485 I/O lines, as well as extended temperature (-40° to 85°C) models are also available.

Acromag, Wixom, MI. (248) 624-1541. [www.acromag.com].

## Development Board Aids Power Supply Design

Because each military and avionics application requires slightly different power conversion needs, custom power supply designs are the norm. Serving that need, Microchip Technology has announced the dsPICDEM Buck Switch-Mode Power Supply (SMPS) Development Board, which comes with sample software and exercises to help designers quickly evaluate and develop digital SMPS and power-conversion products. The new board is populated with a dsPIC30F2020 Digital Signal Controller (DSC) and is supported by Microchip's world-class development tools, as well as a series of educational WebSeminars on digital SMPS-related topics.

The dsPIC30F2020 DSC on the new board implements two of four possible independent, synchronous Buck converter circuits to allow designers to examine digital-power control techniques, as well as application performance indicators such as transient response. Onboard user potentiometers enable simulation of application features such as trim, remote-voltage sense, voltage tracking and current sharing. A CD is included with hands-on digital power-conversion training exercises, and example Buck-converter software comes with the board to help designers quickly adapt digital power to their designs. The dsPICDEM Buck SMPS Development Board (Part # DM300023) is priced at $149.99 each.

Microchip Technology, Chandler, AZ. (480) 792-7200. [www.microchip.com].

## Rugged Case Targets 17-inch Laptops

Laptop computers have become an indispensable tool for warfighters. They often used as the human interface terminals for a variety of complex communications and intelligence gear. Helping keep those laptops safe and secure in the field, Pelican Products has introduced the 1495 Laptop Case. With nearly 1,000 cubic inches of usable storage space, the 1495 can protect all sizes of laptops up to 17" and hold accessories such as power cables, digital storage drives and other electronics. The 1495 also features an integrated, programmable combination lock and stainless-steel-reinforced padlock protectors for twice the theft prevention.

Like all Pelican Protector Cases, the 1495 Laptop Case is engineered with a high-impact, structural resin, and an open cell-core wall construction that protects sensitive equipment from some of the harshest conditions known to man. Additional standard features include a lid equipped with a polymer o-ring for a dust and waterproof seal, dual action latches that have been tested to a failure threshold of nearly 400 pounds (but open with a light pull) and an automatic Gore-Tex pressure equalization valve that prevents vacuum lock, making the case easier to open at any altitude. The deluxe 1495 Laptop Case CC #1 includes all available features and has an MSRP of $309.95.

Pelican Products, Torrance, CA. (310) 326-4700. [www.pelican.com].

## Remote Power Controller Reduces Weight, Cost/Channel

Military engineers developing high-performance power distribution systems with high channel counts and a wide range of current ratings are always looking to reduce price per channel and weight, as well as simplify the development process. The RP-26000 Remote Power Controller from Data Device Corp. was designed to meet all of these needs. With up to 16 user-programmable channels, the RP-26000 series substantially reduces weight and cost per channel compared to mechanical contactors and single-channel solid-state power controller (SSPC) modules. Individual channels of the same current rating can be paralleled to increase single-channel current capacity, allowing flexibility in power management system design.

The card's maximum current-carrying capability is 160A. DSP technology enables intelligent processing power: each channel's controls and current ratings can be set independently. BIT provides continuous status reports. Communication protocols include CANbus, RS 232, RS 422, and RS 485. The card's mechanical design complies with MIL STD 475, commonly used in ground vehicle and aircraft environmental requirements. It is conformal-coated to provide moisture resistance and designed to withstand rugged military extremes of temperature (-40° to +85°C), humidity, vibration and EMI. Pricing for one is $4,500.

Data Device Corp., Bohemia, NY. (631) 567-5600. [www.ddc-web.com].

## Gen2 PCI Express Link Trainer Qualifies PCIe Systems

Companies developing PCI Express Gen2 products that need a controllable host or device running at 5 Gbit/s speeds will appreciate a new card-based development tool from LeCroy that works in tandem with the company's PCI Express PETracer Gen2 Summit Analyzer. The Gen2 PCI Express LinkUP Trainer gives PCI Express developers an initial power-on tool in the early stages of system interoperability, and provides a tool for logical physical layer testing for later stages. LinkUP supports both Platform and Endpoint modes, and supports logical link widths from x1 to x16.

PCI Express LinkUP is designed to qualify PCI Express systems through Link Training and Status State Machine (LTSSM) testing. It can generate training sequences at Gen1/Gen2 speeds for lane widths from x1 to x16. Features such as the LTSSM emulator generate protocol traffic to a device or host. The system can be configured to transition to various states and to change speeds to test speed negotiation. In addition, each PCI Express lane's parameters—such as lane skew, polarity and scrambling—can be changed to expose physical layer issues.

LeCroy, Chestnut Ridge, NY. (845) 425-2000. [www.lecroy.com].

## Rugged Mobile Computers Feature GPS

The latest addition to Grayhill Embedded Group's rugged, configurable Custom Mobile Solutions series is the DuraMax base platform featuring GPS and wireless functionality. Based on the Windows CE operating system and the Intel XScale processor, the DuraMax platform also includes a built-in altimeter and compass, industrial-grade ruggedness to withstand harsh and unpredictable environmental conditions, and portable, lightweight, ergonomic design. Standard options include a 3.5-in. display that delivers improved readability over smaller PDAs and handheld devices and is specially treated to maintain brightness and clarity in harsh sunlight, glare and inconsistent lighting.

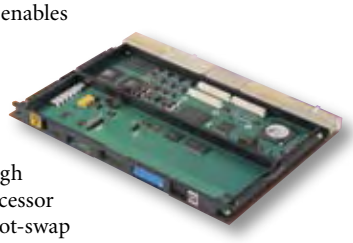
Extended 8- to 10-hour battery life maximizes field functionality between charges, and Secure Digital (SD) and Compact Flash (CF) slots permit increased data storage and linking to an array of specialized peripheral devices that facilitate scanning, printing and photography. The base unit is certified to meet military-grade standards for drops, vibration, humidity, altitude, extreme temperatures, moisture and dust, including MIL-STD-810F and IP67. Grayhill base platforms can be quickly, affordably custom-configured, even at low quantities. Pricing starts at $1,800 for the DuraMax-HG handheld platform with GPS capability.

Grayhill Embedded Group, LaGrange, IL. (800) 217-1305. [www.grayhill.com].

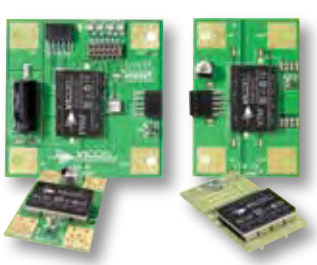
## cPCI Board DeliversExtensive, Flexible I/O for Rugged Apps

Military computing continues to embrace CompactPCI technology, while also demanding more powerful and flexible I/O, a combination that is not easy to find. The rugged CompactPCI MFIO-C6 multi-function I/O card from Radstone Embedded Computing, part of GE Fanuc Embedded Systems, is designed to meet that need. The MFIO-C6 offers a wide range of digital and analog I/O and a low-power MPC8270 PowerQUICC II processor to offload interface management but occupies only a single slot. Features include eight analog inputs, seven open collector 250 mA outputs, forty-eight LVTTL I/O channels, five LVDS output ports, five LVDS input ports, two 10/100BaseT Ethernet channels and six serial ports.

The MFIO-C6's three-axis accelerometer enables tamper detection, and secure instant-erase SRAM destroys the contents automatically at power-off or as a result of a key event. The MPC8270 PowerQUICC II processor supports integral BIT diagnostics, initializes interfaces and manages I/O through a shared memory scheme to reduce host processor loading. The board supports CompactPCI hot-swap mechanisms and provides a number of system-level functions such as an elapsed time indicator, real-time clock and temperature sensor. Pricing begins at $3,700.



Radstone Embedded Computing, part of GE Fanuc Embedded Systems, Billerica, MA. (800) 368-2738. [www.radstone.com].



## Evaluation, Validation Boards Available for V•I Chip Power Components

Factorizing DC/DC power conversion into its basic functions maximizes distributed power system performance and cost-effectiveness. V•I Chip Factorized Power Architecture (FPA) power components from Vicor let engineers do exactly that: isolation and transformation in the voltage transformation modules (VTMs) and regulation in the pre-regulator modules (PRMs). Unregulated bus converter modules (BCMs) complete the lineup. Now the company has launched a line of 52 evaluation and validation boards to help engineers become familiar with the technology quickly and easily.

Four PRM non-isolated regulator boards and 13 VTM current multiplier boards are available. A PRM board that matches desired input voltage is plugged together with a VTM board that provides desired output voltage and current. Fourteen 48V BCM evaluation boards with fixed ratio outputs from 1.5V to 48 VDC are also available, along with high-voltage, 352 Vin and 384 Vin versions. In addition, 21 BCM validation boards with standard 1/4 brick pinning let engineers test the performance of the BCM intermediate bus converter in existing applications and enable 300W or 600W solutions. The evaluation boards are equipped with test sockets, trim pots and convenient input and output connections. Pricing begins at $99 each.

Vicor, Andover, MA. (800) 735-6200. [www.vicorpower.com].

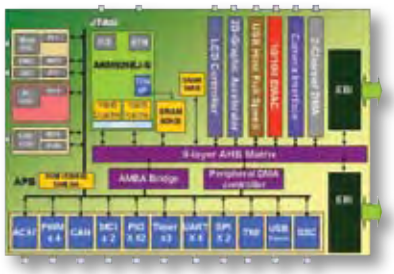
## FC Interface Delivers 4 Gbit/s, ATCA AMC.1 Hot-Swap

Next-generation military computer systems need high levels of online maintainability. To meet that need, Critical I/O has introduced a Fibre Channel interface that delivers 4 Gbit/s connectivity to ATCA systems and provides hot-swap capability via its compliance with the ATCA Advanced Mezzanine Card standard (AMC.1 with PCI Express host interface). The Model FCA2460 AMC Host Bus Adapter module has two independent 4 Gbit/s FC interfaces that, when combined, achieve sustained data rates of 1.5 Gbytes/s, 10 microsecond RDMA data transfers and up to 300,000 SCSI I/O operations per second.

The Model FCA2460 AMC also provides a four-lane PCI Express host interface, full hot-swap capabilities and extensive integrated hardware BIT. It is compatible with X86 and PowerPC ATCA processor blades and is software compatible with the company's PMC and XMC Fibre Channel interfaces. The module is supported by a full complement of library and drivers for VxWorks, Linux and Windows. Pricing is $1,995 in production quantities.

Critical I/O, Irvine, CA. (949) 553-2200. [www.criticalio.com].

## MCU Combines Bandwidth, Networking, Human Interface



Subsystems designed for graphically interfaced, data-intensive military applications such as GPS navigation need lots of networking and human interface peripherals. They also depend on the processing power of 32-bit cores. But much of that compute power can get lost in architectures that don't provide enough bandwidth. Atmel's AT91SAM9263 microcontroller provides a wealth of human interface and networking peripherals, and solves the bottleneck problem with a total on-chip bandwidth of 41.6 Gbits/s, 11 buses, 27 DMA channels and two external bus interfaces. On-chip human interface peripherals include camera, TFT/STN LCD controller, six-channel audio front end (AC'97), I2S and a 2-D graphics coprocessor.

Networking peripherals include 10/100 Fast Ethernet MAC, 1 Mbit/s control area network (CAN), four USARTS, two 50 Mbit/s SPI, CompactFlash and SDIO interface, and a two-wire interface that can be connected to external wired and wireless communication modules such as a GPRS modem and Wi-Fi. Support for external mass storage devices is provided by a USB host, a SD/MMC memory card interface and a dual external bus interface. The AT91SAM9263 is available in a 324-ball ball grid array package priced at under $10 each in quantities of 100,000.

Atmel, San Jose, CA. (408) 441-0311. [www.atmel.com].

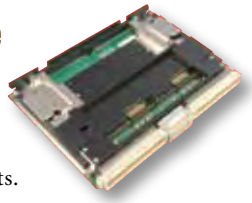
## Rugged 3U CompactPCI SBC Targets Extreme Environments

If there's one thing military systems need it's the ability to operate under extreme temperature conditions. That's why Aitech's C900 series of 3U CompactPCI SBCs provide the industry's widest operating temperature range of -55° to +85°C. The latest in the series, the thermally managed C903, generates all specialty power onboard and uses integral temperature sensors to self-monitor temperature and power dissipation. Powered by a 600 MHz 750FL PowerPC, the C903 comes in air- or conduction-cooled versions. Memory includes up to 1 Gbyte of fast ECC DDR SDRAM, 128 Mbytes of user flash, 64 Mbytes of boot flash, up to 2 Gbytes of NAND flash file memory and 128 Kbytes of NVRAM.

A Marvell MV64460 Discovery III system controller features two separate, independent PCI-X bus interfaces and dual Gigabit Ethernet ports. The board's I/O includes two independent Gigabit Ethernet ports, two high-speed serial communications ports, two USB 2.0 ports, up to eight GPIO and a PMC slot. The C903 features a JTAG/COP interface for debugging and development, test and diagnostic firmware that includes boot software, an AIMon monitor/debugger tool, an AIDiag diagnostic tool and BIT. Board support packages are available for VxWorks and Integrity. Quantity pricing starts at $3,790

Aitech Defense Systems, Chatsworth, CA. (888) 248-3248. [www.rugged.com].

## FPGA-Based DSP VME Engine Is Conduction-Cooled



Demanding signal processing applications require survivability in harsh environments throughout the full range of military application environments. To meet that need, Curtiss-Wright has introduced conduction-cooled rugged versions of its CHAMP FX DSP 6U VME64x and VITA-41 engines. The high-performance IP blocks included in the company's CHAMPtools-FX Design Kit, including I/O logic blocks for SRAM and SDRAM memory controllers, the PCI interface and serial controllers, have also been qualified for use over the entire Level 200 (-40° to 85°C) temperature range.

The CHAMP-FX's FPGA computing power is complemented with I/O speeds of more than 10 Gbytes/s implemented with high-speed differential serial RocketIO, XMC/PMC sites and StarFabric interfaces. The FPGAs have more than 8 Gbytes/s of memory bandwidth from the board's DDR SDRAM and fast DDR-2 SRAM. The conduction-cooled rugged versions meet Curtiss-Wright's Level 100 (-40° to 71°C) and Level 200 ruggedization guidelines, which fully address use in high shock and vibration environments. They are constructed with a hybrid aluminum/copper frame that provides mechanical stiffening while conducting heat from the electronic components to the edge of the card, where it is transferred to the chassis. Prices start at $36,000. Volume discounts are available.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwcembedded.com].

## PCI/PCI-X Boards and PMC Modules Sport Virtex-5 LX FPGA

Deployed signal processing applications will get a big boost from the high-speed serial capabilities of the Virtex-5 LX FPGA from Xilinx. VMetro has released the first Virtex-5 FPGA-based PCI/PCI-X and PMC board-level products for applications such as electro-optics, electronic warfare, SIGINT and telecommunications for high-performance aerospace/defense applications. The DEV-FPGA05 PCI/PCI X boards and PMC-FPGA05 PMC modules are the first in a line of Virtex-5-based boards from VMetro.

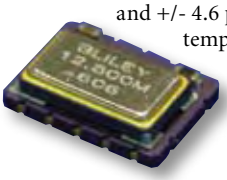
The boards include a Xilinx XC5VLX110 FPGA and multiple banks of QDR SRAM and DDR2 SDRAM. The additional memory helps maximize the FPGA's performance by storing large data sets such as frame buffers for imaging applications, FFTs and lookup tables. Provided Windows software includes utilities for configuring the FPGA and flash memory as well as high-speed PCI-X DMA support. VMetro's Virtex-5-based products start at $6,195.

VMetro, Houston, TX. (281) 584-0728. [www.vmetro.com].

## Crystal Oscillator Targets Wireless/Wireline Mil Comms Apps

The challenge for many designers of military wireless and wireline communication equipment is to provide smaller, cost-effective designs without compromising performance. A new temperature-compensated, voltage-controlled crystal oscillator (TCVCXO) from Bliley Technologies, the T85B Stratum III TCVCXO, provides high-frequency stability in a small, 5 mm x 7 mm, industry-standard ceramic surface-mount package.

The latest in its series of TCVCXO products, the RoHS-compliant T85B's specifications include +/- 0.28 ppm frequency stability over temperature and +/- 4.6 ppm frequency stability over all conditions (20 years of aging). Operating frequency range is 5 MHz to 52 MHz and operating temperature range is -40° to +85°C. Options include CMOS or optional Clipped Sine Wave outputs, 3.3V or 5V power supply and optional voltage-controlled frequency tuning. The Stratum III TCVCXO is a configure-to-order product. Pricing begins at less than $5, depending on configuration.




Bliley Technologies, Erie, PA. (814) 838-3571. [www.bliley.com].

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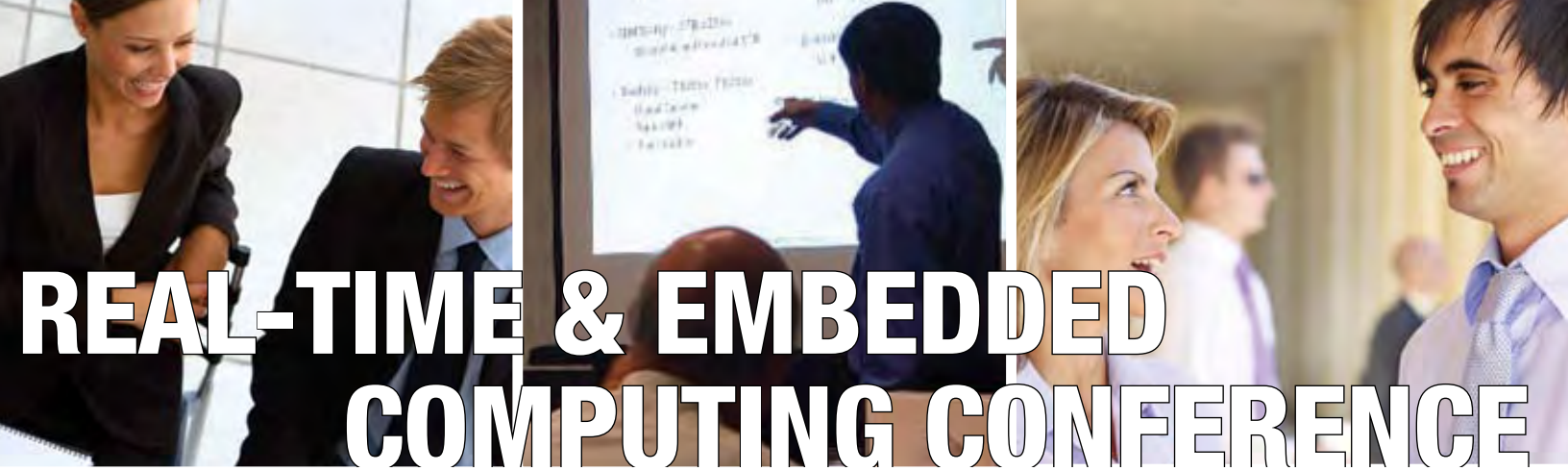

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# Coming Next Month

COTS JOURNAL

- *Rugged Displays.* Leveraging cutting-edge graphics chips developed for the demanding gaming market, military graphics subsystems are now able to offer complex video and graphics functionality in highly integrated board-level solutions. Cockpit displays and simulation/training applications rank as two of the most demanding users of these advanced graphics technologies. Articles in this section examine the graphics solutions available in PMC and other form-factors.
- *ATCA, MicroTCA and AMC Do Defense Duty.* As military applications push for more integrated and small footprint electronics, MicroTCA is gaining interest as a solution, using the growing selection of AMC mezzanine cards essentially as slot cards. ATCA meanwhile, although created for the telecom industry, is gaining a foothold in defense system designs. Articles in this section examine the latest trends along those lines, as well as update on where these technologies fit in current military programs.
- *Test & Analysis for RoHS.* For the general commercial electronics industry, the European Union's RoHS initiative is a hurdle already mounted. Not so for the defense industry. The military market may be exempt from the restriction of hazardous substances (RoHS) initiative, but that doesn't mean makers of board-level products, for example, are off the hook. In this age of COTS, most companies craft board designs targeted for both military and non-military markets. Even companies purely in the military market can't escape RoHS's effects because for some categories of components lead-free versions are the only game in town. This section examines the test and analysis issues that complicate military system design in this era of RoHS.
- *Data Acquisition Boards.* Driven by the twin trends toward higher sensor performance and the inclination to tie more sensors together into wider arrays, makers of high-end data acquisition boards and subsystems are designing the latest A/D converters into board-level system architectures. These board architectures are leveraging FPGAs as a means to efficiently channel digitized data. This Tech Focus section updates readers on those trends and provides a product album of representative data acquisition board products across a variety of form factors—including VME, cPCI, USB, PCI Express and more.

# Editorial

Jeff Child, Editor-in-Chief

# A Box by Any Other Name …

Sometimes a technology trend can sneak up on you. If you can get past my poor play on that famous Shakespearean line in the title of this editorial, I'll proceed to examine what is now an entrenched product category in the military embedded computing arena: stand-alone rugged boxes. The trend toward vendors in the embedded computer market offering ever more complete systems is nothing new. It's been steadily gaining steam for the past 6 to 8 years actually. But within the last 12 months the concept has really become a fixture in this market.

Before I go any further let me define what I mean by stand-alone rugged boxes. They typically comprise a set of modular embedded boards housed in a rugged enclosure that has its own power supply and interface ports to link to a variety of user terminals. Often the boards in the box are standards-based cards such as PC/104, PMC and 3U CompactPCI. But the enclosures by and large aren't in any industry standard footprint, although that may change as standards like MicroTCA and VITA 56 gain acceptance in the military realm. I'm not talking about ATR enclosures—although those continue to be a main staple of many military and avionics systems. I'm talking about the general category of complete integrated, rugged box-level systems. These are typically sold as a complete working system, often with some degree of environmental testing done beforehand by the vendor. The system is typically designed to work as stand-alone, plugged into whatever I/O and user interface scheme meets the application need.

The stand-alone rugged box trend is separate from the strategy know as "appliqué," whereby complete computer units—like rugged laptops—are applied or woven onto existing weapons platforms and integrated with government-furnished software. In some sense, stand-alone rugged boxes are a competing trend to appliqué because they overlap somewhat as solutions.

At present, there are at least 12 companies that I know of in our marketplace that now have some sort of stand-alone rugged box-level system in their offerings—many even have whole product lines in that category. As I said, these kinds of systems aren't new in the sense that many suppliers have offered just such integrated systems as a custom, customer-specific solution—usually driven by the requirements handed down from a prime or sub-prime contractor. What's changed is that now customers can choose from a variety of these boxes and procure them as standard products. Honestly, until last summer we didn't really have a handle on what to call these systems. That's no knock against us. The industry itself has no consistent term for them.

Each summer, the RTC Group editorial team gets together for a key planning meeting where we decide what areas we're going to focus on the next year. It takes some serious crystal ball forecasting to effectively decide in July 2006 what the hot trends will be throughout the entirety of 2007. Because electronics and embedded computing technology can shift drastically within 12 months, we sometimes need to add or subtract a few topics that are on the current year's editorial calendar. This was the case with stand-alone rugged boxes.

At our summer meeting we struggled to come up with an accurate name for that product category. After some back and forth, we settled on the term "Stand-Alone Rugged Boxes" and decided to add it to our editorial calendar as a "mid-season replacement" (to put it in television jargon). With that in mind, our Senior Editor Ann Thryft put together a brilliant section on this topic in our November issue of *COTS Journal.* We must have been on target selecting it as an important trend, because in her research, Ann discovered it was indeed a rich topic and timely. Much of what's driving it, she learned, comes from the current war effort. The push is to minimize size, weight and power, while cramming in more Gflops per watt to boost the processing muscle in smaller UAVs and unmanned ground vehicles (UGVs), and on larger platforms such as JSTARS.

Now that we've identified this product category as a critical area important to our readers, expect to see it covered often throughout this year—not only as a specific topic, but also within various sections that we've always covered. In other words, stand-alone rugged boxes will be examined in terms of thermal issues, power conversion, processing architectures, I/O strategies and so on—always, of course, in the context of their use in military system designs.

Stand-alone rugged boxes will factor big in two of the in-depth supplements we have planned this year, targeting two dynamic areas of military technology. The first is on UAV Payloads. Both new and existing UAV programs are demanding greater levels of onboard processing muscle. The UAV Payloads supplement will examine the enclosure, board architectures and fabric solutions that match up with the needs of various UAV payload requirements. Our second supplement will be on Vetronics (vehicle electronics). The sophistication of onboard communications and control electronics is expected to multiply for both next-generation and Current Force fighting vehicles. The supplement will look at those developments as well as the technologies and solutions critical for Vetronics.

As we enter our ninth year of publication, we're committed to pushing *COTS Journal* to the next level in order to stay in tune with and ahead of the critical technologies driving today's military programs. Please join us for the ride. ▮▮

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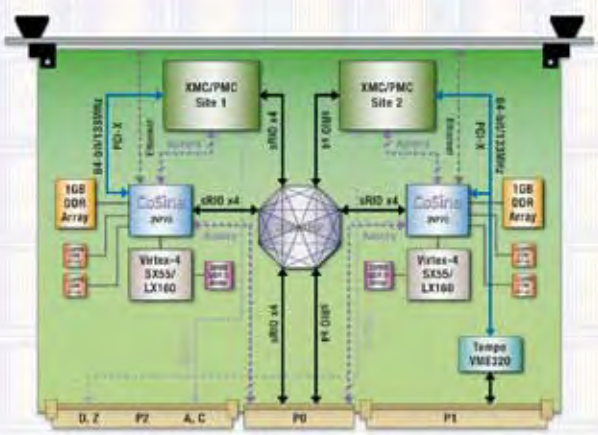


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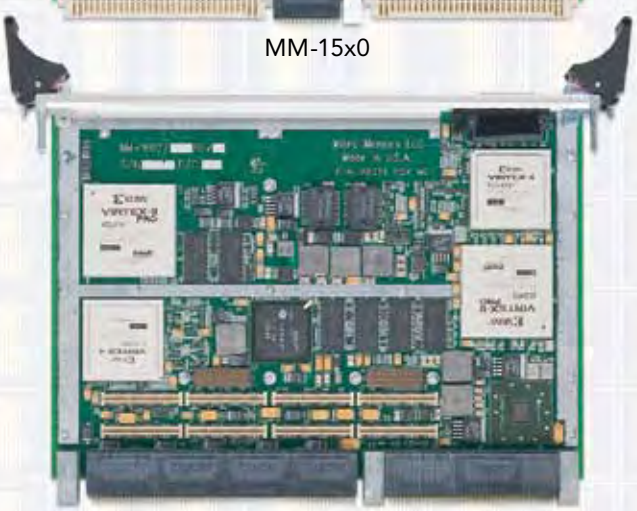

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